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New Approach for Defining the Threshold Voltage of MOSFETs

J. A. Salcedo, A. Ortiz-Conde, F. J. García Sánchez, J. Muci, J. J. Liou, and Y. Yue

Abstract—The threshold voltage of MOSFETs has traditionally been defined as the gate voltage required to cause the surface potential to be equal to twice the Fermi potential in the bulk of semiconductor. Such a definition, although widely used for modeling long-channel MOSFET's, becomes increasingly questionable for modern devices with diminishing channel lengths. In this paper a new approach is proposed which defines the threshold voltage based on the intersection of the two asymptotes of the surface potential for the depletion and strong inversion regions. The approach is tested in simulation environment for MOS devices having different channel lengths, oxide thicknesses, and substrate doping concentrations.

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I. INTRODUCTION

The threshold voltage, V_T , is a very important device parameter for the design, modeling, simulation and utilization of MOSFET's [1]–[5]. It is common in the literature to define V_T as the gate voltage at which the surface potential at the Si–SiO₂ interface becomes twice the Fermi potential in the bulk of semiconductor [2]. Attempts have been made in the past to improve this definition [6], [7]. For example, a definition was reported recently [7] to take into account the effects of depletion charges in the channel of the MOSFET. Such a definition improves the accuracy of the V_T model for long-channel devices, but its improvement is less significant for MOSFETs with a channel length in the sub-micron range.

A new approach for defining the threshold voltage, which is valid for both long- and short-channel devices, is proposed here. It is based on

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concept that the threshold occurs at the intersection of the two asymptotes of surface potential for the depletion and strong inversion regions. The validity of the approach is verified using results simulated from MOS devices with various doping densities, channel lengths, and oxide thicknesses. The values of V_T predicted by this new approach are compared with those predicted by existing definitions and obtained from two extraction methods which determine V_T from the drain current versus gate voltage characteristics [8]–[13]. Quantum-mechanical effects, which may be important for deep-submicron MOSFETs, will not be considered in the present study.

II. THRESHOLD VOLTAGE DEFINITIONS FOR LONG CHANNEL DEVICES

For an n-channel MOSFET, the relationship between the surface potential and the gate voltage can be written as follows [2], [3]:

$$V_{GS} - V_{FB} = \psi_S \pm \frac{\epsilon_s}{C_o} (F^2(\psi_S))^{1/2} \quad (1)$$

where the minus sign is used when the bands bend up, the plus sign is used when the bands bend down, V_{GS} is the gate-to-source voltage, ψ_S is the surface potential, C_o is the oxide capacitance, V_{FB} is the flatband voltage, and F is the Kingston function [2]:

$$F^2(\psi_S) \equiv \frac{2}{\beta^2 L_D^2} \cdot \left[(e^{-\beta\psi_S} + \beta\psi_S - 1) + \frac{n_o}{p_o} (e^{\beta\psi_S} - \beta\psi_S - 1) \right]. \quad (2)$$

Here, $\beta = q/kT$ is the inverse of the thermal voltage, p_o and n_o are the equilibrium hole and electron densities, and L_D is the extrinsic Debye length

$$L_D = \left(\frac{\epsilon_s}{q\beta p_o} \right)^{1/2}. \quad (3)$$

In (2), the terms $\exp(-\beta\psi_S)$, $(\beta\psi_S - 1)$, and $(n_o/p_o) [\exp(\beta\psi_S) - \beta\psi_S - 1]$ are associated with the accumulation, depletion, and inversion charges, respectively.

The conventional definition states that the threshold voltage is the gate voltage which produces a surface potential equal to twice the Fermi potential, ϕ_B , in the bulk of semiconductor. According to this definition, the surface potential at threshold, dubbed here the threshold surface potential, ψ_{ST} , can be expressed as

$$\psi_{ST} \equiv 2\phi_B \equiv \frac{1}{\beta} \ln \left(\frac{p_o}{n_o} \right) \equiv \frac{2}{\beta} \ln \left(\frac{N_A}{n_i} \right), \quad (4)$$

where n_i is the intrinsic free-carrier concentration and N_A is the substrate doping density.

This conventional definition for the threshold surface potential can be derived as follows. Using the condition that $\beta\psi_S$ is much larger than unity at the onset of strong inversion, the second term inside the brackets in (2), which is associated with the inversion charge, can be approximated by

$$\frac{n_o}{p_o} (e^{\beta\psi_S} - \beta\psi_S - 1) \approx \frac{n_o}{p_o} e^{\beta\psi_S} = e^{\beta(\psi_S - 2\phi_B)}. \quad (5)$$

For the onset of strong inversion, this term must be larger than unity. Hence, equating this to unity, (5) becomes

$$e^{\beta(\psi_{ST} - 2\phi_B)} = 1, \quad (6)$$

which yields $\psi_{ST} = 2\phi_B$, as stated in (4). Substituting this value into (1) results in the conventional analytic expression for the threshold voltage of long-channel MOSFETs (henceforth referred to as “the conventional definition”).

Because this conventional definition does not agree well with V_T extracted from the drain current versus gate voltage characteristics, Tsividis [6] proposed to improve the definition by adding an empirical term to the threshold surface potential to account for second-order effects. The value proposed for this additional term is about $6/\beta$, for a typical range of substrate doping concentrations and oxide thickness, so that

$$\psi_{ST} \approx 2\phi_B + \frac{6}{\beta}. \quad (7)$$

Substituting this threshold surface potential into the equation relating the gate voltage to the surface potential yields an empirical expression for the threshold voltage (henceforth referred to as “the empirical definition”).

Another modification to the definition of threshold voltage for long-channel devices was developed based on comparing the inversion and depletion charge terms described in (2), which has the following expression [7]:

$$\beta\psi_{ST} \approx 2\beta\phi_B + \ln\left(\frac{2\beta\phi_B}{\zeta}\right) \quad (8)$$

where ζ is also an empirical parameter with a value of about 10 for a typical range of substrate doping concentration and oxide thickness. Substitution of this modified threshold surface potential expression into ψ_S versus V_{GS} curve results in another definition for the threshold voltage of long-channel devices (henceforth referred to as “the modified definition”). The distinction between this and the conventional and empirical definitions lies in the term $\ln(2\beta\phi_B/\zeta)$ in (8), which depends on the depletion charges. In other words, $\zeta = 2\beta\phi_B$ was used implicitly in the conventional definition, whereas $\ln(2\beta\phi_B/\zeta) = 6$ was used in the empirical definition given in (7).

III. NEW APPROACH FOR DEFINING THRESHOLD VOLTAGE

The new approach for defining threshold voltage takes into consideration the surface potential asymptotic behavior of both the depletion and strong inversion regions to determine the threshold surface potential. Before proceeding, let us introduce a new variable, ψ_i , called the intrinsic surface potential, which will be used instead of ψ_S to simplify the procedure. This variable defines the surface potential with respect to the intrinsic Fermi level in the bulk of semiconductor:

$$\psi_i \equiv \psi_S - \phi_B. \quad (9)$$

Using this variable, (1)–(3) can be re-written as

$$V_{GS} - V_{FB} - \phi_B = \psi_i \pm V_o \left(G^2(\psi_i)\right)^{1/2}, \quad (10)$$

where G is a modified expression of the Kingston function

$$G^2(\psi_i) \equiv e^{-\beta\psi_i} + e^{\beta\phi_B}(\beta\psi_i + \beta\phi_B - 1) + e^{\beta\psi_i} - e^{-\beta\phi_B}(\beta\psi_i + \beta\phi_B + 1) \quad (11)$$

and

$$V_o \equiv \frac{2kT\varepsilon_s n_i}{C_o}. \quad (12)$$

For the case of n -channel devices, using (9)–(12), and considering the corresponding dominant terms for each bias condition, we can ob-

tain equations that define the asymptotes of (10) in three regions of operation:

$$V_{GS} - V_{FB} - \phi_B \approx \psi_i + V_o e^{(\beta\psi_i/2)} \quad (13)$$

for strong inversion,

$$V_{GS} - V_{FB} - \phi_B \approx \psi_i - V_o e^{(-\beta\psi_i/2)} \quad (14)$$

for accumulation, and

$$V_{GS} - V_{FB} - \phi_B \approx \psi_i + V_o e^{(\beta\phi_B/2)} [\beta\psi_i + \beta\phi_B - 1]^{1/2} \quad (15)$$

for depletion.

The advantage of using ψ_i to describe the surface potential can be illustrated by analyzing its characteristics in strong inversion and accumulation. For very strong inversion [i.e., $V_{GS} - V_{FB} \gg \phi_B$ and $V_o \exp(\beta\psi_i/2) \gg \psi_i$], (13) can be approximated by

$$\psi_i \approx \frac{2}{\beta} \ln\left(\frac{V_{GS} - V_{FB}}{V_o}\right). \quad (16)$$

Analogously, for very strong accumulation [i.e., $V_{GS} - V_{FB} \ll \phi_B$ and $V_o \exp(-\beta\psi_i/2) \gg \psi_i$], (14) can be approximated by

$$\psi_i \approx -\frac{2}{\beta} \ln\left(-\frac{V_{GS} - V_{FB}}{V_o}\right). \quad (17)$$

Note that the values of ψ_i in (16) and (17) are equal but opposite to each other (i.e., symmetrical).

Based on the concept that the onset of inversion lies at the transition between the depletion and strong inversion regions, with verification given later, we propose that the intersection of the strong-inversion and depletion surface potential asymptotes [(13) and (15)] can be used to define accurately the threshold voltage of MOSFET's. The value of ψ_i at this intersection represents the threshold surface potential, ψ_{iT} , and the corresponding value of V_{GS} is the threshold voltage V_T (henceforth referred to as “the asymptotic definition”). The concept of this intersection, which does not have an explicit expression for V_T , can be used to define V_T for both the long- and short-channel MOSFETs. The two asymptotes cannot be calculated directly from (13) and (15), however; they are obtained by fitting the two equations to the simulated or measured ψ_i versus V_{GS} characteristics with ϕ_B and V_o as fitting parameters. Second-order effects, such as short-channel effects, are readily imbedded in the simulated or measured data and thus are accounted for in the asymptotic definition.

For the case of long-channel MOSFETs, an analytic model for the threshold voltage can also be derived based on this asymptote intersection concept, which is given below. An analytic expression for the threshold surface potential of long-channel MOSFETs can be found by solving (13) and (15):

$$\psi_{iT} = \phi_B + \frac{\ln(\beta\psi_{iT} + \beta\phi_B - 1)}{\beta}. \quad (18)$$

Substitution of (18) into (15) gives the asymptotic definition of V_T for long-channel MOSFET's. However, such an expression would not be computationally convenient since ψ_{iT} exists on both the left- and the right-hand-side of (18). An approximated expression can be obtained by noting that since at threshold ψ_{iT} is close to ϕ_B , it can be substituted by ϕ_B in the argument of the logarithm without appreciable loss of accuracy. Therefore, the threshold voltage can be expressed as

$$V_T \approx V_{FB} + 2\phi_B + \frac{\ln(2\beta\phi_B - 1)}{\beta} + V_o e^{(\beta\phi_B/2)} [2\beta\phi_B + \ln(2\beta\phi_B - 1) - 1]^{1/2}. \quad (19)$$

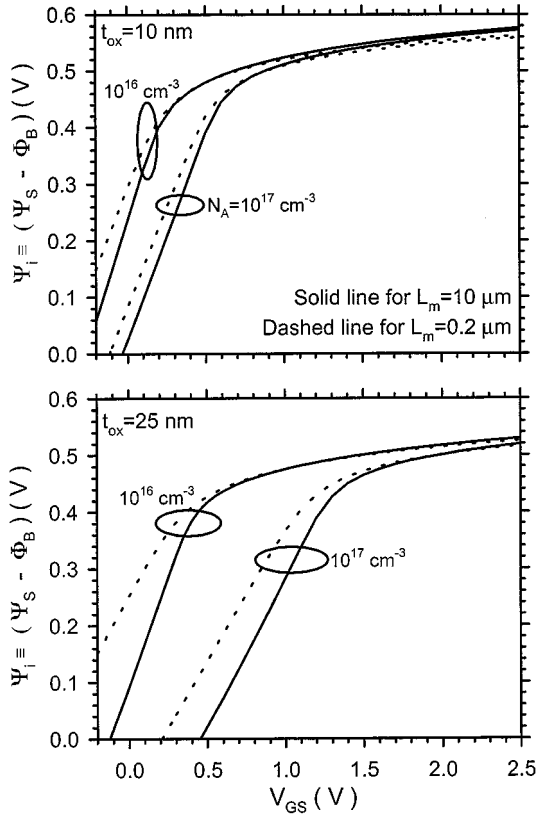


Fig. 1. Simulated intrinsic surface potential versus gate voltage characteristics of long- and short-channel MOSFETs having two oxide thicknesses and two substrate doping densities.

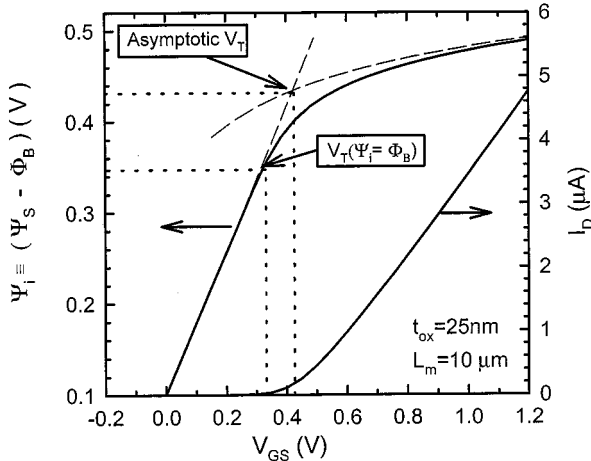


Fig. 2. Simulated intrinsic surface potential and drain current as a function of gate voltage for a long-channel MOSFET ($L_m = 10 \mu\text{m}$, $t_{ox} = 25 \text{ nm}$, $N_A = 10^{16} \text{ cm}^{-3}$). The values of threshold voltage predicted by the intersection of the two surface potential asymptotes and by the conventional definition are indicated.

We can further simplify (19) to a more compact form by considering that, for substrate doping densities in the range of 10^{14} to 10^{18} cm^{-3} , the term $\ln(2\beta\phi_B - 1)$ has a value between 2.8 and 3.5. Using an intermediate value of three for this term in (19) we obtain the following approximated expression for V_T (henceforth referred to as “the approximate asymptotic definition”):

$$V_T \approx V_{FB} + 2\phi_B + \frac{3}{\beta} + V_o e^{(\beta\phi_B/2)} [2(\beta\phi_B + 1)]^{1/2}. \quad (20)$$

TABLE I
THRESHOLD VOLTAGE OBTAINED FROM TWO EXTRACTION METHODS
AND PREDICTED BY VARIOUS DEFINITIONS FOR LONG-CHANNEL
DEVICES WITH $L_m = 10 \mu\text{m}$

Values of V_T		$t_{ox}=25 \text{ nm}$		$t_{ox}=10 \text{ nm}$	
		$N_A[\text{cm}^{-3}] = 10^{16}$	10^{17}	10^{16}	10^{17}
Extracted from I_D vs. V_{GS}	Linear Extrapolation	0.43	1.32	0.22	0.62
	Second Derivative	0.43	1.33	0.22	0.62
Predicted By Definitions	Conventional: V_{GS} at $\psi_{ST} \approx 2\phi_B$	0.33	1.25	0.14	0.52
	Empirical: V_{GS} at ψ_{ST} given by Eq. (7)	0.50	1.43	0.28	0.70
	Modified: V_{GS} at ψ_{ST} given by Eq. (8)	0.37	1.35	0.17	0.58
	Present Asymptotic: V_{GS} at ψ_{IT} given by intersection of the two asymptotes	0.43	1.32	0.22	0.62
	Present Approximate Asymptotic: given by Eq. (20)	0.42	1.29	0.20	0.62

It is clear that the analytic expression in (20) is applicable only for long-channel devices. However, the approach of defining threshold at the intersection of the strong-inversion and depletion surface potential asymptotes [(13) and (15)] is valid for both the long- and short-channel devices. This will be demonstrated in the next section.

IV. RESULTS AND DISCUSSIONS

Long and short n-channel MOSFETs are simulated using the two-dimensional device simulator MICROTREC [14] to verify the new V_T approach developed in the previous section. The device structure under study has heavily doped n^+ -type source and drain regions with a peak doping concentration of 10^{20} cm^{-3} , a junction depth of $0.05 \mu\text{m}$ with a lateral extent of $0.015 \mu\text{m}$, and a contact width of $0.5 \mu\text{m}$. The separation between the source- and drain-contact to the gate is $0.5 \mu\text{m}$. Two mask channel lengths L_m of 0.2 and $10 \mu\text{m}$, three gate oxide thicknesses t_{ox} of 5 , 10 and 25 nm , and two substrate doping concentrations N_A of 10^{16} and 10^{17} cm^{-3} are considered. The gate work function is 4.35 eV , and the semiconductor electron affinity is 4.17 eV .

Fig. 1 presents the simulated ψ_i versus V_{GS} characteristics for short and long-channel devices with different substrate doping concentrations and oxide thicknesses at a zero drain-source voltage V_D . The simulation results were taken at the Si-SiO₂ interface and in the middle of the channel. Two different asymptotic behaviors can be observed in this figure: a) $\psi_i \propto V_{GS}$ for depletion, which agrees with (15); and b) $\psi_i \propto \ln(V_{GS})$ for strong inversion, which follows (13). The values of ψ_i for very strong inversion are independent of substrate doping concentration, thus suggesting that using ψ_i instead of ψ_S is a more convenient and universal way to visualize the surface potential behavior and to define the threshold voltage. This figure also indicates that the strong inversion asymptotes are weakly dependent on channel length and that the behavior of the depletion asymptotes for short-channel devices is analogous to their long-channel counterpart.

Fig. 2 illustrates simulated ψ_i versus V_{GS} behavior for a long-channel device with $L_m = 10 \mu\text{m}$, $t_{ox} = 25 \text{ nm}$, $N_A = 10^{16} \text{ cm}^{-3}$, together with the two asymptotes of ψ_i corresponding to the strong inversion and depletion regions. The projection of the intersection of the two asymptotes on the V_{GS} -axis yields a value of $V_T = 0.43 \text{ V}$ (denoted as “Asymptotic V_T ” in the figure). The value of V_T predicted using the approximate asymptotic formula given in (20) is 0.42 V . On the other hand, the conventional definition suggested

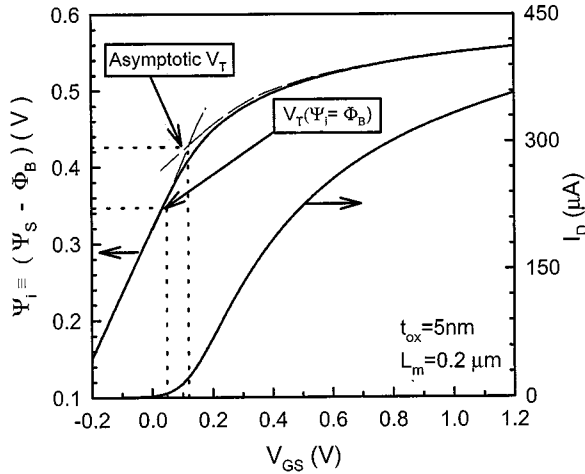


Fig. 3. Simulated intrinsic surface potential and drain current as a function of gate voltage for a short-channel MOSFET ($L_m = 0.2 \mu\text{m}$, $t_{ox} = 5 \text{ nm}$, $N_A = 10^{16} \text{ cm}^{-3}$). The values of threshold voltage predicted by the intersection of the two surface potential asymptotes and by the conventional definition are indicated.

a lower value of 0.33 V [denoted as “ $V_T(\psi_i = \phi_B)$ ” in the figure]. The I_D versus V_{GS} characteristics, measured at a small V_D of 0.05 V, is also included in the figure. From this curve, a value of $V_T = 0.43$ V is extracted using either the linear extrapolation or the second derivative extraction method. Clearly, the threshold voltage predicted by the present approach is in better agreement with that extracted from current–voltage (I – V) curve than the conventional definition.

Fig. 3 shows the results for a short-channel device with $L_m = 0.2 \mu\text{m}$, $t_{ox} = 5 \text{ nm}$, $N_A = 10^{16} \text{ cm}^{-3}$. The value of V_T extracted from the I_D versus V_{GS} characteristics measured at $V_D = 0.05 \text{ V}$ is 0.10 V. The threshold voltage predicted by the conventional definition is only 0.05 V, whereas a value of 0.12 V is predicted by the present asymptotic definition based on the intersection of the two asymptotes. Note that the approximate asymptotic definition [(20)] does not apply for this device.

To provide a more comprehensive comparison, Table I lists V_T values for long-channel devices obtained from the different methods. It is shown that among the V_T values predicted by the several different definitions, the asymptotic definition yields the best match to the extracted values of V_T . The approximate asymptotic formula offers a simpler but slightly less accurate way of defining the threshold voltage. The conventional and empirical definitions underestimate and overestimate the threshold voltage, respectively, and the modified definition provides a small improvement over these two definitions. The same trend is observed in Table II, which summarizes the values of V_T for short-channel devices. Again, among all the definitions considered, the asymptotic definition yields the most accurate results.

It should be pointed out that the surface potential, and thus ψ_i , is a function of the position in the channel and the drain voltage V_D , and such dependencies increase with decreasing channel length. While the theory presented in the paper applies generally, the middle of the channel and $V_D = 0$ have been used in the simulation of ψ_i and extraction of the asymptotic V_T . The use of mid-point in the channel can be justified by the reasoning that this position is least influenced by the electric fields associated with the source/drain junctions (i.e., the minimum surface potential is near the center of the channel) and can thus best represent the behavior of inversion in the channel. This is supported by the results in Fig. 4, which indicates that the minimum potential is located near the center of the channel even for a 0.2 μm device with $V_D = 0.1 \text{ V}$. To verify the use of zero V_D , we show in Fig. 5 ψ_i versus V_{GS} characteristics simulated for a 0.2- μm MOS and three

TABLE II
THRESHOLD VOLTAGE OBTAINED FROM TWO EXTRACTION METHODS AND PREDICTED BY VARIOUS DEFINITIONS FOR SHORT-CHANNEL DEVICES WITH $L_m = 0.2 \mu\text{m}$

Values of V_T		$t_{ox}=25 \text{ nm}$		$t_{ox}=10 \text{ nm}$		$t_{ox}=5 \text{ nm}$	
		$N_A [\text{cm}^{-3}] = 10^{16}$	10^{17}	10^{16}	10^{17}	10^{16}	10^{17}
Extracted from I_D vs. V_{GS}	Linear Extrapolation	0.26	1.12	0.13	0.49	0.10	0.27
	Second Derivative	0.26	1.15	0.15	0.50	0.10	0.30
Predicted by Definitions	Conventional: V_{GS} at $\psi_{ST} \approx 2\phi_B$	0.21	1.05	0.09	0.43	0.05	0.21
	Empirical: V_{GS} at ψ_{ST} given by Eq. (7)	0.40	1.28	0.24	0.61	0.25	0.40
	Modified: V_{GS} at ψ_{ST} given by Eq. (8)	0.29	1.22	0.12	0.55	0.07	0.32
	Present Asymptotic: V_{GS} at ψ_{IT} given by intersection of the two asymptotes	0.29	1.16	0.16	0.52	0.12	0.32

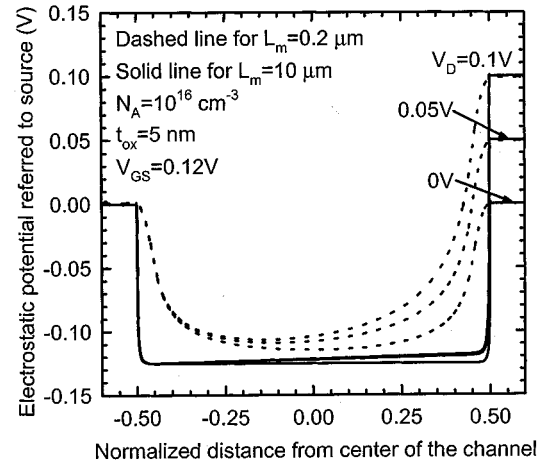


Fig. 4. Simulated electrostatic potentials versus the normalized position in the channel of long-channel (solid lines) and short-channel (dashed lines) MOS devices with three different drain voltages.

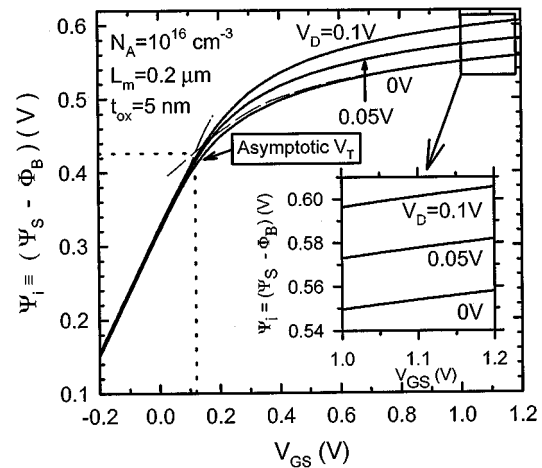


Fig. 5. Simulated intrinsic surface potential for a short-channel MOSFET and three different drain voltages.

different small V_D . Clearly, asymptotic V_T determined is insensitive to the different V_D considered. This suggests that the error associated with

using zero V_D in extracting asymptotic V_T is minimal. A final note is that V_T extracted in this paper is intended for the threshold voltage of strong inversion, and a different V_T may be needed for characterizing the onset of subthreshold region.

V. CONCLUSIONS

Design and modeling of submicron MOSFETs require an accurate theoretical definition for the threshold voltage V_T . A new approach for defining V_T has been proposed based on the intersection of the surface potential asymptotes for the depletion and strong inversion regions. It was shown that the threshold voltage defined by such an approach offers a better agreement with V_T extracted from the drain-current versus gate-voltage characteristics than those predicted by the conventional and other modified definitions. In particular, it was demonstrated in the device simulation environment that the new approach provides a greater accuracy than other existing definitions for both long- and short-channel MOSFETs having various oxide thicknesses and substrate doping densities.

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Deuterium Isotope Effect for AC and DC Hot-Carrier Degradation of MOS Transistors: A Comparison Study

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Abstract—Several new phenomena are observed comparing the ac stress with the dc stress. In the initial stress period (< 30 s), the deuterium isotope effect is smaller for ac stress than for dc stress, which is ascribed to the hole injection. In the final stress stage ($> 10^4$ s), the saturation of the G_m degradation stops and the G_m degradation starts to increase again for ac stress, which is probably due to the hole trapping.

Index Terms—CMOS, deuterium, hot-carrier, reliability.

I. INTRODUCTION

The discovery of the giant deuterium isotope effect in hot-carrier degradation of MOS transistors has fueled the industrial development of the use of this effect to improve the reliability of integrated circuits [1]–[8]. On the other hand, the deuterium isotope effect can be used as an effective tool to help solve the long-standing mystery of hot-carrier degradation mechanisms in MOS transistors [9]–[11]. Some researchers suggested that the degradation is caused by both hole and electron injection into the oxide [12]–[14]. Recently, we showed direct experimental evidence to support the new theory that the dominant degradation mechanism is the direct interaction of hot electrons with Si–H/D bonds [9]–[11]. All of the above hot-carrier degradation experiments are carried out in dc stress. However, MOS transistors in real integrated circuits work in an ac dynamic environment. It is very important to study the deuterium isotope effect for devices under ac stress. In addition, the role of holes in the isotope effect is not very clear. In order to collect more evidence, we study the ac stress with the gate pulsed from 0 to 3 V, because more holes are injected in this bias. In this brief, we report for the first time, the study of the deuterium isotope effect in ac hot-carrier degradation.

In the experiments, 0.35- μm 3.3 V n-MOS transistors with a gate oxide of 65 Å were used. The devices consist of phosphorus-implanted LDD source and drain, oxide spacers, and three levels of metallization. The devices were annealed in 100% H_2 or 100% D_2 in conventional furnace (one atmosphere) for 3 h. During the ac stress, the drain was connected to a constant voltage of 5.5 V, while the gate was pulsed between 0 V and 3 V with a pulse period of 2 μs , a pulsewidth of 1 μs , and both the rise and fall times of 100 ns. In order to compare the ac stress with the dc stress, the dc stress was carried out in similar devices and duty cycles of the ac stress were considered. For the dc stress, the transistors are stressed at $V_D = 5.5$ V and $V_G = 3$ V (maximum I_{sub}). In order to assure that holes are injected into the oxide region above the channel outside the drain, V_D should be larger than the critical drain voltage V_D^* [14]. In our case, the critical drain voltage V_D^* was found to be 5.2 V. We found that under the condition of $V_D = 5.5$ V and $V_G = 0.6$ V, the maximum hole injection was produced. Therefore, we chose $V_D = 5.5$ V for the ac and dc stress. The degradation tests

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