

# A Method to Extract Mobility Degradation and Total Series Resistance of Fully-Depleted SOI MOSFETs

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**Abstract**—Free-carrier mobility degradation in the channel and drain/source series resistance are two important parameters limiting the performance of MOS devices. In this paper, we present a method to extract these parameters from the drain current versus gate voltage characteristics of fully-depleted (FD) SOI MOSFETs operating in the saturation region. This method is developed based on an integration function which reduces errors associated with the extraction procedure and on the d.c. characteristics of MOS devices having several different channel lengths. Simulation results and measured data of FD SOI MOSFETs are used to test and verify the method developed.

**Index Terms**—Mobility degradation, parameter extraction, series resistance, SOI MOSFETs, threshold voltage, velocity saturation.

## I. INTRODUCTION

ACCURATE parameter extraction becomes increasingly important and critical for device modeling, particularly for modern MOS devices with feature size approaching  $0.1 \mu\text{m}$ . Considerable research work [1]–[15] has been dedicated to this subject in the past ten years. Two of the most important parameters for MOS device characterization and circuit simulation are the free-carrier mobility degradation in the channel and drain/source series resistance [4]–[8]. Mobility degradation will give rise to an effect similar to that of the drain/source series resistance on the current–voltage ( $I$ – $V$ ) characteristics [2], and Katto has suggested [3] that such an effect can be modeled as a series resistance. McAndrew and Layman [4] used nonlinear optimization to extract these two parameters, but their approach is not physics based and the extracted values may not have any physical meaning. Methods based on evaluating derivatives of the drain current have also been

Manuscript received April 27, 2001; revised September 17, 2001. This work was supported by Universidad Simón Bolívar, by CONICIT (Venezuela) Grant S1–98000567, and by CONACYT (Mexico) Project N134400-A. The review of this paper was arranged by Editor C. McAndrew.

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Publisher Item Identifier S 0018-9383(02)00236-8.

proposed [5]–[7], but using the derivatives has the disadvantage of enhancing the effect of noise on parameter extraction. Lim and coworkers [8] have proposed to measure the devices by adding an external resistance, which requires additional circuit components and complicates the extraction procedure.

In this paper, we will first show that, from the saturation drain current ( $I_{\text{Dsat}}$ ) versus gate voltage ( $V_{\text{gs}}$ ) characteristics, the mobility degradation effect can be modeled as an effective resistance in series with the drain/source resistance. Second, we will develop a method to extract the total effective resistance and the transconductance parameter from the  $I_{\text{Dsat}}$ – $V_{\text{gs}}$  characteristics. This method is based on a mathematical concept developed previously [13]–[18], which uses integrations, instead of differentiation, to minimize the effect of experimental noise and error associated with the parameter extraction procedure. Finally, we will apply the method to fully-depleted (FD) SOI MOSFETs having several different channel lengths to extract the total series resistance and the mobility degradation. SOISPICE [19] simulation, ATLAS [20] device simulation, and measured data will be presented to support and validate the extraction method.

## II. DEVELOPMENT OF PARAMETER EXTRACTION METHOD

Consider an n-channel FD SOI MOSFET operating in the saturation region and under strong inversion. The gate and drain terminals are connected together to ensure saturation operation. The saturation drain current may be expressed as [12], [13], [21], [22]

$$I_{\text{Dsat}} = \frac{K}{2} (V_{\text{GS}} - V_T)^2 \quad (1)$$

where  $V_T$  is the threshold voltage

$$V_{\text{GS}} = V_{\text{gs}} - I_{\text{Dsat}} R_s \quad (2)$$

is the intrinsic gate-source voltage,  $V_{\text{gs}}$  is the extrinsic gate-source voltage,  $R_s$  is the source series resistance

$$K = \frac{K_o}{1 + \theta (V_{\text{GS}} - V_T)} \quad (3)$$

is the transconductance parameter with a unit of  $\text{A} \cdot \text{V}^{-2}$ . In (2),  $\theta$  is the mobility degradation parameter

$$K_o = \frac{W \mu_o C_o}{L_{\text{eff}} (1 + \alpha)} \quad (4)$$

is the low-field transconductance parameter,  $\alpha$  is the parameter that accounts for the charge coupling effects between front and

back interfaces [21], [22],  $\mu_o$  is the low-field mobility,  $C_o$  is the oxide capacitance,  $L_{\text{eff}}$  is the effective channel length, and  $W$  is the channel width.

It is important to point out that a very large drain/source series resistance could take the device out of the saturation region even if the drain and gate terminals are connected together (i.e.,  $V_{\text{ds}} = V_{\text{gs}}$ ). In general, the saturation condition requires  $V_{\text{ds}} > V_{\text{gs}} - V_T$ . For the case of  $V_{\text{ds}} = V_{\text{gs}}$  and accounting for the voltage drops in the drain/source resistance, the saturation condition becomes  $V_T > I_{\text{Dsat}} R_d$ .

Substituting (2) and (3) into (1) and solving for  $V_{\text{gs}}$ , we obtain

$$V_{\text{gs}} = V_T + R_t I_{\text{Dsat}} + \left( \frac{2I_{\text{Dsat}}}{K_o} + R_\theta^2 I_{\text{Dsat}}^2 \right)^{1/2} \quad (5)$$

where

$$R_\theta \equiv \frac{\theta}{K_o} \quad (6)$$

is an effective resistance due to the free-carrier mobility degradation in the channel, and

$$R_t \equiv R_s + R_\theta \quad (7)$$

is the total effective resistance.

To simplify the analysis, we employ the following condition:

$$\frac{2I_{\text{Dsat}}}{K_o} \gg R_\theta^2 I_{\text{Dsat}}^2. \quad (8)$$

This can be rewritten by substituting (1), (3), and (6) into (8) and performing some algebraic manipulations, which leads to

$$2.73 \gg \theta (V_{\text{GS}} - V_T). \quad (9)$$

For typical SOI MOSFETs,  $\theta$  is much smaller than unity, and the inequality in (9) is usually valid. Putting (8) into (5) yields

$$V_{\text{gs}} \approx V_T + R_t I_{\text{Dsat}} + \left( \frac{2}{K_o} \right)^{1/2} I_{\text{Dsat}}^{1/2}. \quad (10)$$

Based on an approach developed previously [13]–[18], we propose to use the following function to suppress the linear term of  $I_{\text{Dsat}}$  in (10):

$$G_1(V_{\text{gs}}, I_{\text{Dsat}}) = V_{\text{gs}} - \frac{2}{I_{\text{Dsat}}} \int_0^{V_{\text{gs}}} I_{\text{Dsat}}(V_{\text{gs}}) dV_{\text{gs}}. \quad (11)$$

The function defined in (11), with a unit of V, can be numerically computed from the simulated or measured  $I_{\text{Dsat}}(V_{\text{gs}})$  characteristics. Using integration by parts, (11) becomes

$$G_1(V_{\text{gs}}, I_{\text{Dsat}}) = \frac{2}{I_{\text{Dsat}}} \int_0^{I_{\text{Dsat}}} V_{\text{gs}}(I_{\text{Dsat}}) dI_{\text{Dsat}} - V_{\text{gs}}. \quad (12)$$

Then, by substituting (10) into (12) and performing the integration,  $G_1$  can be evaluated analytically to yield

$$G_1(V_{\text{gs}}, I_{\text{Dsat}}) = V_T + \frac{1}{3} \left( \frac{2}{K_o} \right)^{1/2} I_{\text{Dsat}}^{1/2}. \quad (13)$$

Therefore, the value of  $K_o$  can be obtained from the slope of  $G_1$  versus  $I_{\text{Dsat}}^{1/2}$  plot, and  $V_T$  can be determined from the intercept of the linear extrapolation of the  $G_1$  curve to the y-axis. Knowing  $K_o$  and  $V_T$ ,  $R_t$  can be obtained using the following equation derived from (10):

$$R_t \approx \frac{V_{\text{gs}} - V_T - \left( \frac{2}{K_o} \right)^{1/2} I_{\text{Dsat}}^{1/2}}{I_{\text{Dsat}}}. \quad (14)$$

We summarize the extraction procedure developed so far. It basically consists of the following three steps: a) calculating  $G_1(I_{\text{Dsat}}^{1/2})$  using the simulated or measured  $I_{\text{Dsat}}(V_{\text{gs}})$  characteristics; b) extracting the values of  $K_o$  and  $V_T$  from the plot of  $G_1(I_{\text{Dsat}}^{1/2})$  using (13); and c) evaluating  $R_t$  using (14).

The procedure described above to extract  $K_o$ ,  $V_T$ , and  $R_t$  can be repeated for different mask channel lengths. As will be shown below, this step can be used to determine the individual values of  $\theta$  and  $R_s$ . From (4), the linear dependence of  $K_o^{-1}$  on  $L_{\text{eff}}$  is given by

$$K_o^{-1} = \frac{L_{\text{eff}}(1 + \alpha)}{W \mu_o C_o}. \quad (15)$$

Combining (4), (6), and (7), we obtain  $R_t$  as a function of  $L_{\text{eff}}$ :

$$R_t \equiv R_s + \theta \frac{(1 + \alpha) L_{\text{eff}}}{W \mu_o C_o}. \quad (16)$$

This indicates that  $R_t$  is linearly dependent of  $L_{\text{eff}}$  when the second term in the right hand side of (16) is dominant, and that  $R_t$  approaches  $R_s$  if the second term is negligible. Note that the effective channel length is related to the mask channel  $L_m$  length by

$$L_{\text{eff}} \equiv L_m - \Delta L \quad (17)$$

where  $\Delta L$  is effective channel-length reduction, which can be estimated from the  $K_o^{-1}$  versus  $L_m$  curve [13]. Finally, we can substitute (4) into (16) to obtain

$$R_t \equiv R_s + \theta K_o^{-1}. \quad (18)$$

Equation (18) therefore provides a simple way to extract  $\theta$  from the slope, and  $R_s$  from the vertical axis intercept, of the  $R_t$  versus  $K_o^{-1}$  plot. For most MOSFETs, the drain and source are symmetrical, and the total drain/source series resistance is  $R_d + R_s \approx 2R_s$ .

Now, let us include the velocity saturation effect in the above analysis, and for simplicity let us assume that there is no mobility degradation. Therefore, (1) and (2) are still valid, and (3) should be replaced by

$$K = \frac{K_o}{1 + \frac{V_{\text{ds}}}{L_{\text{eff}} \epsilon_{\text{sat}}}} \quad (19)$$

where

$$\varepsilon_{\text{sat}} = \frac{v_{\text{sat}}}{\mu_o} \quad (20)$$

is the saturation (or critical) electric field and  $v_{\text{sat}}$  is the saturation velocity. Comparing (3) to (19), together with  $V_{\text{ds}} = V_{\text{gs}}$  (i.e., drain and gate are connected together), we obtain a parameter  $\theta_{\text{sat}}$  resulting from the velocity saturation effect:

$$\theta_{\text{sat}} = \frac{1}{L_{\text{eff}} \varepsilon_{\text{sat}}}. \quad (21)$$

Since  $\theta_{\text{sat}}$  is a function of  $L_{\text{eff}}$ , it is better to model it as an effective series resistance  $R_{\text{sat}}$  due to the velocity saturation effect:

$$R_{\text{sat}} = \frac{\theta_{\text{sat}}}{K_o}. \quad (22)$$

Combining (4) and (20)–(22), we obtain

$$R_{\text{sat}} = \frac{(1 + \alpha)}{W C_o \mu_o \varepsilon_{\text{sat}}} = \frac{(1 + \alpha)}{W C_o v_{\text{sat}}}. \quad (23)$$

Including this resistance, the total effective resistance becomes

$$R_t \equiv R_s + R_{\text{sat}} + \theta K_o^{-1}. \quad (24)$$

The slope of the  $R_t$  versus  $K_o^{-1}$  plot yields  $\theta$ , and the intercept of  $R_t$  versus  $K_o^{-1}$  plot to the vertical axis gives the value of  $(R_s + R_{\text{sat}})$ .

### III. VALIDATION USING SOISPICE SIMULATIONS

The new extraction procedure was first applied to the simulation results of SOISPICE [19] for fully-depleted, grounded back-gate SOI MOSFETs. The parameters used are a channel width of 10  $\mu\text{m}$ , mask channel length of 10  $\mu\text{m}$ , front gate oxide thickness of 5.6 nm ( $C_o = 6.16 \times 10^{-7}$  F/cm<sup>2</sup>), back gate oxide thickness of 395 nm, film (body) thickness of 40 nm, film (body) doping density of  $3.8 \times 10^{17}$  cm<sup>-3</sup>, source/drain doping density of  $5 \times 10^{19}$  cm<sup>-3</sup>, LDD region length of 0.1  $\mu\text{m}$  with a doping density of  $5 \times 10^{19}$  cm<sup>-3</sup>, effective channel-length reduction of 0.8  $\mu\text{m}$ , low-field mobility of 600 cm<sup>2</sup>/V·s, mobility degradation coefficient of  $10^{-6}$  cm·V<sup>-1</sup>, saturation velocity of  $6 \times 10^6$  cm/s, and the rest of the parameters as given in the example “fd.idvg.nmod.in” in [19]. It is important to point out that the mobility degradation coefficient used in SOISPICE is related to but is not the same as the parameter  $\theta$  used in this work. The drain/source series resistance was defined externally to the device, and the model’s internal parasitic resistance was set to zero. The drain and gate terminals were connected together to ensure saturation operation, and it is assumed  $R_d = R_s$ .

Fig. 1 shows the simulated  $I_{\text{Dsat}}$  versus  $V_{\text{gs}}$  characteristics of FD SOI MOSFETs with a channel length of 10  $\mu\text{m}$  and three values of  $R_d = R_s$ . As expected, the current decreases with increasing drain/source resistance. Fig. 2 presents the  $G_1$  versus  $I_{\text{Dsat}}^{1/2}$  plot obtained from the  $I$ - $V$  characteristics given in Fig. 1. It is important to point out that  $G_1$  is exactly the same for the three values of  $R_d = R_s$ , suggesting that it is independent of

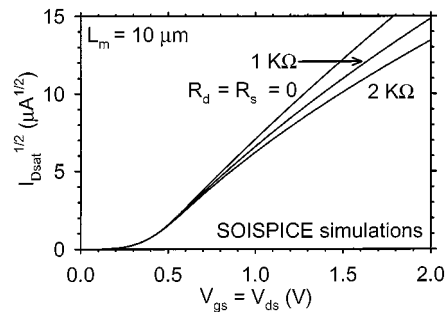


Fig. 1. SOISPICE simulated drain saturation current versus gate bias for a FD SOI MOSFET with a channel length of 10  $\mu\text{m}$  and three different drain/source series resistances.

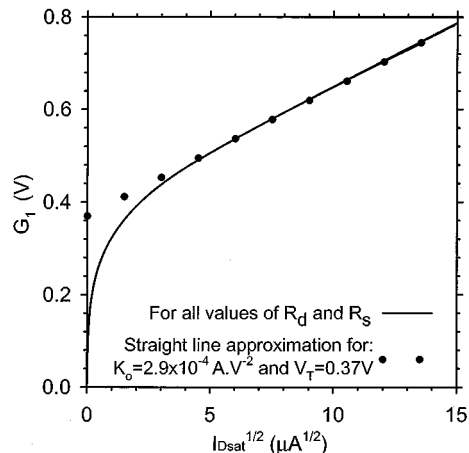


Fig. 2. Function  $G_1(V_{\text{gs}})$  calculated (solid line) based on the  $I$ - $V$  characteristics illustrated in Fig. 1. The closed circles are the linear fit to the  $G_1$  curve. Notice that  $G_1$  is independent of the drain/source series resistance and that it is linearly dependent of  $I_{\text{Dsat}}^{1/2}$  in the strong inversion region.

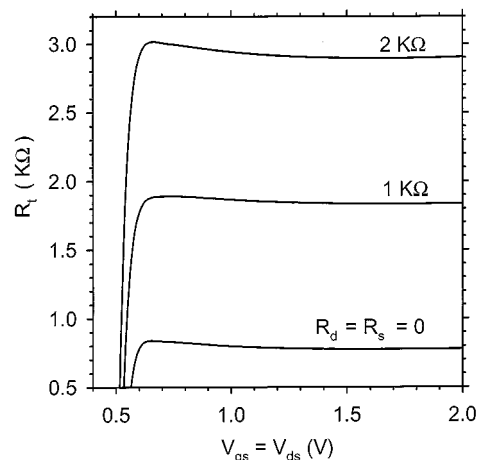


Fig. 3. Extracted values for the total effective resistance bias for the three drain/source resistance cases.

the series resistance. Notice also that for the strong inversion region,  $G_1$  is linearly dependent of  $I_{\text{Dsat}}^{1/2}$ , as indicated in (13). From the slope we obtain  $K_o = 2.9 \times 10^{-4}$  A·V<sup>-2</sup>, and from the intercept of the linear part of the  $G_1$  plot (i.e., strong inversion) to the vertical axis we obtain  $V_T = 0.37$  V.

Fig. 3 shows  $R_t$  versus  $V_{\text{gs}}$  extracted using (14) for the three cases of  $R_d = R_s$ . The region where  $R_t$  is relatively flat is

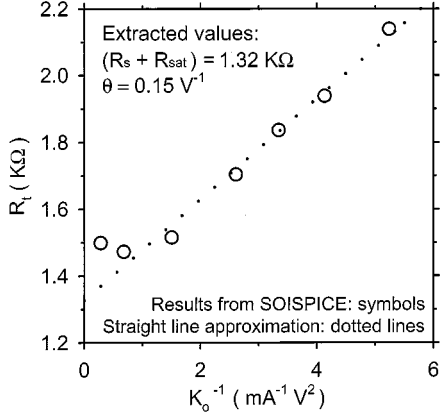


Fig. 4. Total effective resistance (open circles) versus the inverse of the transconductance parameter obtained from SOISPICE simulations for several FD SOI MOSFETs with different channel lengths. The linear fit (dotted lines) allows for the extraction of  $R_s + R_{\text{sat}} = 1.32 \text{ k}\Omega$  and  $\theta = 0.15 \text{ V}^{-1}$ .

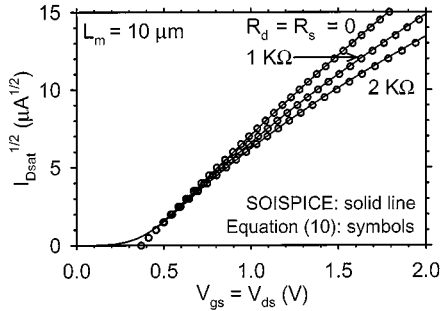


Fig. 5. Comparison of drain saturation current obtained from SOISPICE (solid line) and from the model playback (symbols) using the parameters extracted from the present method.

the strong inversion region; outside this region, where  $R_t$  decreases sharply with decreasing  $V_{\text{gs}}$ , the model and the extraction method developed are not applicable. Since  $R_t$  has three components [ $R_\theta$ ,  $R_s$  and  $R_{\text{sat}}$ , as indicated in (24)], and considering that  $(R_\theta + R_{\text{sat}})$  is the same for the three cases, the difference in  $R_t$  shown in this figure must be the difference in the values of  $R_s$ . Clearly that is the case, since the difference of  $R_s$  agrees very well with that used in the SOISPICE simulation. Also, the extracted value of  $R_t = (R_\theta + R_{\text{sat}}) = 0.78 \text{ k}\Omega$  for the case of  $R_d = R_s = 0$  arises from the effects of mobility degradation and velocity saturation. Knowing the saturation velocity ( $V_{\text{sat}} = 6 \times 10^6 \text{ cm/s}$ ) and using the estimated value of  $\alpha = 0.08$ , we found  $R_{\text{sat}} = 0.29 \text{ k}\Omega$  and  $R_\theta = (R_t - R_{\text{sat}}) = 0.49 \text{ k}\Omega$ . This implies  $\theta = 0.14 \text{ V}^{-1}$ .

Fig. 4 presents  $R_t$  versus  $K_o^{-1}$  extracted from SOISPICE simulation results for several FD SOI MOSFETs having  $R_d = R_s = 1 \text{ k}\Omega$  and different mask channel lengths (2, 3, 5, 8, 10, 12, and 15  $\mu\text{m}$ ). As suggested by (18),  $R_t$  is linearly proportional to  $K_o^{-1}$  for long-channel devices ( $L_m > 5 \mu\text{m}$ ) and is about constant for short-channel devices ( $L_m < 5 \mu\text{m}$ ). In this figure, the open circles are the extracted values and the dotted lines are the linear fit. Then, based on (24), the intercept of the linear fit to the y-axis is  $(R_s + R_{\text{sat}}) = 1.32 \text{ k}\Omega$  and the slope gives  $\theta = 0.15 \text{ V}^{-1}$ . Since  $R_{\text{sat}} = 0.29 \text{ k}\Omega$ , we obtain  $R_s = 1.03 \text{ k}\Omega$ , which is very close to the 1  $\text{k}\Omega$  value

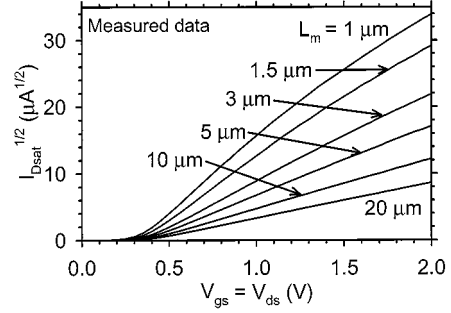


Fig. 6. Measured drain saturation current characteristics of FD SOI MOSFETs having various mask channel lengths.

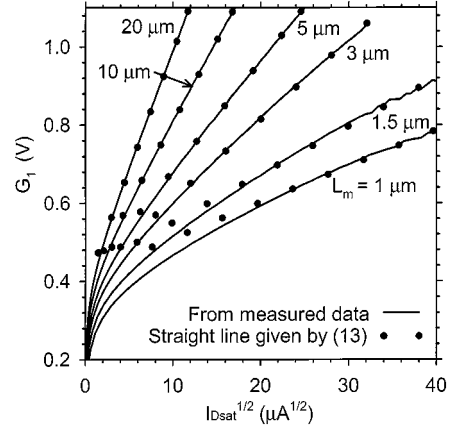


Fig. 7. Integration function  $G_1(V_{\text{gs}})$  calculated (solid lines) from the experimental  $I$ - $V$  characteristics shown in Fig. 6. The closed circles are the straight line fits to the  $G_1$  curves.

used in the SOISPICE simulation. This agreement clearly suggests that the method developed to extract the mobility degradation parameter and drain/source series resistance is accurate and effective. To further verify our method, additional simulations were also carried out using a very high saturation velocity ( $V_{\text{sat}} = 6 \times 10^8 \text{ cm/s}$ ) so that the velocity saturation effect can be assumed negligible. For this case, the intercept yields  $R_s = 1 \text{ k}\Omega$ , as expected.

Fig. 5 compares the  $I$ - $V$  characteristics obtained from SOISPICE and from the FD SOI MOSFET model playback ((1)–(4)) using the parameters extracted from the present method. The values of the parameters are  $V_T = 0.37 \text{ V}$ ,  $K_o = 0.29 \text{ mA} \cdot \text{V}^{-2}$  and  $R_t = 0.78, 1.77, \text{ and } 2.79 \text{ k}\Omega$ . The excellent agreement shown in Fig. 5 verifies again the validity and accuracy of the present extraction method.

#### IV. PARAMETER EXTRACTION FROM MEASURED AND SIMULATED DATA

Several fully-depleted, grounded back-gate SOI MOSFETs fabricated from the same technology were measured as well. The device make-ups are as follows: a channel width of 20  $\mu\text{m}$ , front gate oxide thickness of 30 nm, back gate oxide thickness of 400 nm, film (body) thickness of 80 nm, and mask channel lengths varying from 1 to 20  $\mu\text{m}$ . Measured  $I_{\text{Dsat}}$  versus  $V_{\text{gs}}$  characteristics for the various channel lengths are presented in Fig. 6. Fig. 7 shows  $G_1$  versus  $I_{\text{Dsat}}^{1/2}$  curves based on the  $I$ - $V$

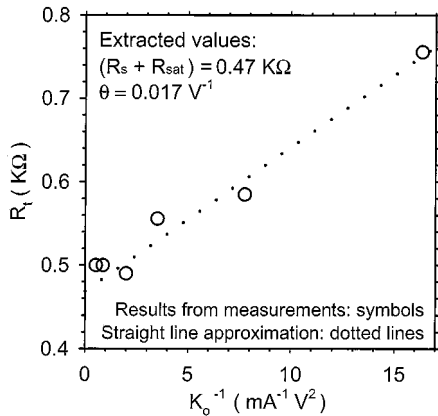


Fig. 8. Total effective resistance (open circles) versus the inverse of the transconductance parameter obtained from the experimental data. The linear fit (dotted lines) allows for the extraction of  $R_s + R_{\text{sat}} = 0.47 \text{ k}\Omega$  and  $\theta = 0.017 \text{ V}^{-1}$ .

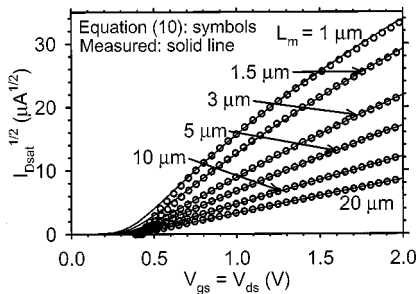


Fig. 9. Comparison of drain saturation current obtained from measurements (solid line) and from the model playback (symbols) using the parameters extracted from the present method.

characteristics in Fig. 6. For the strong inversion region,  $G_1$  is linearly dependent of  $I_{\text{Dsat}}^{1/2}$ , and we can extract  $K_o$  from the slope and  $V_T$  from the intercept to the vertical axis.

Fig. 8 presents the  $R_t$  versus  $K_o^{-1}$  plot obtained from the  $G_1$  curves given in Fig. 7 for several devices with different mask channel lengths (1, 1.5, 3, 5, 10, and 20  $\mu\text{m}$ ). This, together with (18), yields  $(R_s + R_{\text{sat}}) = 0.47 \text{ k}\Omega$  and  $\theta = 0.017 \text{ V}^{-1}$ . Using the estimated value of  $R_{\text{sat}} = 0.29 \text{ k}\Omega$ , we obtain  $R_s = 0.18 \text{ k}\Omega$ .

Fig. 9 compares the  $I$ - $V$  characteristics obtained from measurements and from the model playback using the extracted parameters. Very good agreement is found in the strong inversion region where the model and the extraction method are applicable.

As shown in the previous figures, none of the SOI devices available to us has a mask channel length below 1  $\mu\text{m}$ . To further verify the validity of the proposed method for devices in the submicron range, we have also carried out simulations using ATLAS device simulator [20] for SOI devices with mask channel lengths of 0.3, 0.4, and 0.5  $\mu\text{m}$  and having the same device make-ups as the 1- to 20- $\mu\text{m}$  devices considered earlier. To ensure simulation accuracy, the device simulator was calibrated against the measured characteristics of the previously considered SOI devices. Fig. 10 presents the drain saturation current characteristics of these short-channel devices obtained from ATLAS simulations and from the model playback using

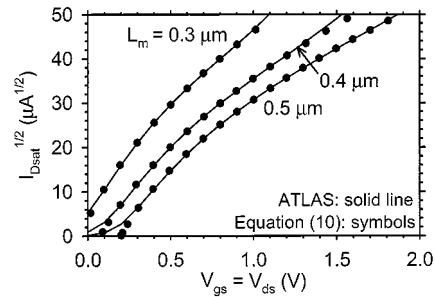


Fig. 10. Current-voltage characteristics as a function of gate bias of three short-channel SOI devices obtained from ATLAS simulations (solid line) and from model playback (symbols) using the extracted parameters.

the above extracted parameters. Again, good agreement is observed for the submicron devices.

## V. CONCLUSION

Free-carrier mobility degradation, velocity saturation, and drain/source series resistance are important factors limiting SOI MOSFET performance. It has been shown that both mobility degradation and velocity saturation effects can be modeled as effective resistances in series with the drain/source resistance. A method has been developed to extract these parameters based on an integration function applied to the drain saturation current characteristics. The accuracy of the method has been verified against results obtained from SOISPICE and ATLAS simulations for fully-depleted SOI MOSFETs down to 0.3  $\mu\text{m}$  mask channel length. Several SOI devices with mask channel lengths varying from 1 to 20  $\mu\text{m}$  have also been considered and measured, and their parameters successfully extracted using the present extraction method.

## ACKNOWLEDGMENT

The authors are grateful to Prof. J. Fossum at University of Florida for providing SOISPICE.

## REFERENCES

- [1] Y. Taur, "MOSFET channel length: extraction and interpretation," *IEEE Trans. Electron Devices*, vol. 47, pp. 160–170, Jan. 2000.
- [2] K. O. Jeppson, "Static characterization and parameter extraction in MOS transistors," *Microelectron. Eng.*, vol. 40, pp. 181–186, 1998.
- [3] H. Katto, "Device parameter extraction in the linear region of MOSFET'S," *IEEE Electron Device Lett.*, vol. 18, pp. 408–410, 1997.
- [4] C. C. McAndrew and P. A. Layman, "MOSFET effective channel length, threshold voltage, and series resistance determination by robust optimization," *IEEE Trans. Electron Devices*, vol. 39, pp. 2298–2311, 1992.
- [5] C. L. Lou, W. K. Chim, D. S. H. Chan, and Y. Pan, "A new DC Drain-current-conductance method (DCCM) for the characterization," *IEEE Electron Device Lett.*, vol. 18, pp. 327–329, 1997.
- [6] —, "A novel single-device DC method for extraction of the effective mobility and source-drain resistances of fresh and hot-carrier degraded drain-engineered MOSFET'S," *IEEE Trans. Electron Devices*, vol. 45, pp. 1317–1323, 1998.
- [7] C. B. Tan, W. K. Chim, D. S. H. Chan, and C. L. Lou, "An improved drain-current-conductance method with substrate back-biasing," *IEEE Trans. Electron Devices*, vol. 46, pp. 431–433, Mar. 1999.
- [8] G. M. Lim, Y. C. Kim, D. J. Kim, Y. W. Park, and D. M. Kim, "Additional resistance method for extraction of separated nonlinear parasitic resistances and effective mobility in MOSFET'S," *Electron. Lett.*, vol. 36, pp. 1233–1234, 1998.

- [9] K. Terada, K. Nishiyama, and K. I. Hatanaka, "Comparison of MOSFET threshold voltage extraction methods," *Solid-State Electron.*, vol. 45, pp. 35–40, 2001.
- [10] A. S. Nicolett, J. A. Martino, E. Simoen, and C. Claeys, "A new method to extract the LDD doping concentration on fully depleted SOI nMOSFET at 300 K," in *Proc. Third IEEE Int. Caracas Conf. on Devices, Circuits and Systems*, 2000, pp. D45/1–D45/5.
- [11] ———, "Extraction of the lightly doped drain concentration of fully depleted SOI NMOSFETS using the back gate bias effect," *Solid-State Electron.*, vol. 44, pp. 677–684, 2000.
- [12] D. K. Schroeder, *Semiconductor Material and Device Characterization*, 2nd ed. New York: Wiley, 1998.
- [13] J. J. Liou, A. Ortiz-Conde, and F. J. García Sánchez, *Analysis and Design of MOSFETS: Modeling, Simulation and Parameter Extraction*. New York: Kluwer, 1998.
- [14] A. Ortiz-Conde, F. J. García Sánchez, and J. J. Liou, "An overview on parameter extraction in field effect transistors," *Acta Científica Venezolana*, vol. 51, pp. 176–187, 2000.
- [15] F. J. García Sánchez, A. Ortiz-Conde, G. De Mercato, J. A. Salcedo, J. J. Liou, and Y. Yue, "New simple procedure to determine the threshold voltage of MOSFETS," *Solid-State Electron.*, vol. 44, pp. 673–675, 2000.
- [16] F. J. García Sánchez, A. Ortiz-Conde, G. De Mercato, J. J. Liou, and L. Recht, "Eliminating parasitic resistances in parameter extraction of semiconductor device models," in *Proc. First IEEE Int. Caracas Conf. on Devices, Circuits and Systems*, 1995, pp. 298–302.
- [17] F. J. García Sánchez, A. Ortiz-Conde, and J. J. Liou, "A parasitic series resistance-independent method for device-model parameter extraction," in *Proc. Inst. Elect. Eng., Circuits, Devices, Syst.*, vol. 143, 1996, pp. 68–70.
- [18] F. J. García Sánchez, A. Ortiz-Conde, G. De Mercato, and J. J. Liou, "Parameter extraction and signal processing using potential functions," *Univ. Cienc. Tecnol.*, vol. 4, pp. 123–136, 2000.
- [19] *SOISPACE (Ver. 5.0) SPICE2 with UFSOI MOSFET Models. User's Guide, SOI Group*, ser. FL 32 611-6130, J.G. Fossum, Ed., Univ. Florida, Gainesville, 1994.
- [20] *ATLAS Manual*, Silvaco International, 1999.
- [21] J. P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*, 2nd ed. Norwell, MA: Kluwer, 1997.
- [22] H. K. Lim and J. G. Fossum, "Current-voltage characteristics of thin-film SOI MOSFET'S in strong inversion," *IEEE Trans. Electron Devices*, vol. ED-31, pp. 401–408, 1984.

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