

Modeling the Undoped-Body Symmetric Dual-Gate MOSFET

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Abstract- A model of the undoped-body symmetric dual-gate MOSFET is presented based on the explicit analytic solution of its surface potential using the Lambert W Function. The total channel carrier charge and drain current may be readily obtained from this solution. Results from the proposed solution are compared to exact results numerically calculated by iteration.

I. INTRODUCTION

The use of symmetric dual-gate (SDG) silicon-on-insulator (SOI) MOSFETs with undoped channel regions is one the most promising emerging technologies for scaling CMOS devices down to nanometer sizes [1]. The absence of dopant atoms in the channel eliminates impurity scattering mobility degradation and completely does away with unwanted dispersion in the characteristics, otherwise resulting from the random microscopic dopant fluctuations inherent to ultra-small dimensions devices. In fact, the threshold voltage is determined by the work function difference between the gate material and the intrinsic silicon body. Such advanced MOSFETs are already being fabricated in several configurations including planar, vertical, FinFET, and various other 3-D geometries [2].

Highly accurate and physics based compact models which are at the same time computationally efficient are required for proper modeling of MOSFETs [3]. These requirements are easier to meet in the case of undoped-body MOSFETs because of the absence of fixed charge in the channel, and even more so in the case of ultra thin-body symmetric DG MOSFETs. Proposed models in general lack computational efficiency since they rely on numerical iteration to solve the fundamental equations [4-7]. An explicit analytic solution is therefore highly desirable because it offers the possibility of greater physical insight and computational efficiency than its numerical alternatives.

To that end we recently proposed [8] an explicit analytic solution for the surface potential of undoped-body single-gate bulk devices making use of the Lambert W function [9], a special function not expressible in terms of elementary functions, which is defined as the solution to the equation $W(x) \exp[W(x)] = x$. The Lambert W function has already proved its usefulness in numerous physics applications and has also been recently utilized for finding the solutions to

several previously unsolved but basic diode [10] and bipolar transistor circuit analysis problems [11]. The use of Lambert function-based device models for circuit simulation applications is facilitated by the fact that this function has already been incorporated into some circuit simulation tools. More recently the Lambert Function solution approach was also introduced to describe the inversion charge of undoped-body symmetric DG MOSFETs [12]. In what follows we present an explicit analytic Lambert Function-based solution of the surface potential of undoped-body symmetric DG devices which is an extension of our previously proposed analytic solution for the surface potential of undoped-body single-gate bulk devices [8]. The total channel carrier charge and drain current will then be formulated from that surface potential solution.

II. POTENTIAL MODELING

Figure 1 presents a schematic structure of a symmetric DG n-MOSFET, where x is the direction across the channel thickness and y is the direction along the channel. Here symmetric means that the two gates have the same work function, the top and bottom gate oxide thicknesses are equal, and the same voltage bias is applied to both gates. It is assumed that the Quasi-Fermi level is constant along the x direction, current flows in the y direction and assumed negligible in the x direction. Because there is no contact to the silicon body, the energy levels are referenced to the electron quasi-Fermi level of the n^+ source, as indicated in Fig. 2.

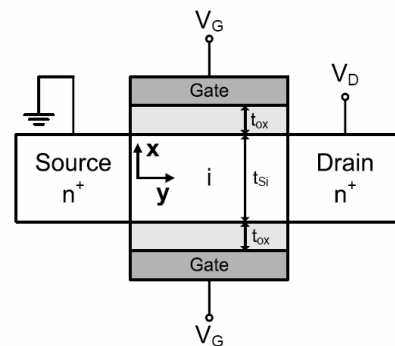


Fig. 1. Schematic structure of a symmetric DG n-MOSFET.

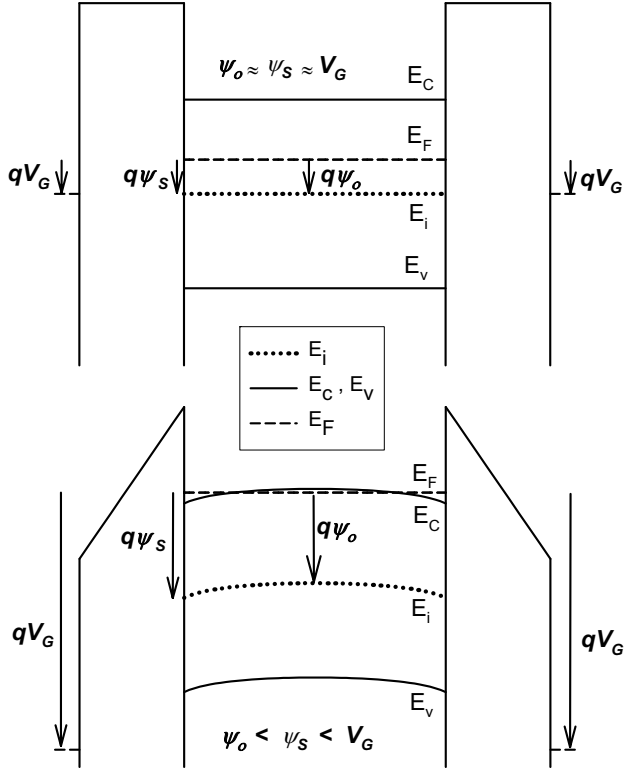


Fig. 2 Undoped-body symmetric DG n-MOSFET channel potential within the channel thickness, at two gate voltage biases, (top) below threshold, and (bottom) above threshold.

For simplicity's sake, the formulation is based on Maxwell-Boltzmann, not on Fermi-Dirac, charge distribution statistics. Quantum confinement effects will not be taken into account here either, although they may be incorporated later to accommodate devices of silicon film thicknesses smaller than 5 nm where these effects start to become relatively significant. A one dimensional Poisson equation across the body thickness of this device can be written as [13, 14]

$$\frac{d^2 \psi}{dx^2} = \frac{q n_i}{\epsilon_s} \left[e^{\beta(\psi - V)} - e^{-\beta\psi} \right] \quad (1)$$

where n_i is the intrinsic carrier density, q is the electronic charge, $\beta = q/kT$ is the inverse of the thermal voltage, ϵ_s is the silicon permittivity, and V is the difference between electron and hole quasi-Fermi levels along the channel (channel voltage), equal to 0 at the source and to V_{DS} at the drain. The mixed boundary conditions at the center of the channel and at its surface are, respectively:

$$\left. \frac{d\psi}{dx} \right|_{x=0} = 0 \quad (2)$$

and

$$V_{GS} - V_{FB} = \psi \left(x = \frac{t_{Si}}{2} \right) + \frac{\epsilon_s}{C_o} \frac{d\psi}{dx} \Big|_{x=\frac{t_{Si}}{2}}, \quad (3)$$

where t_{Si} is the silicon thickness, V_{GS} is the gate-to-source voltage, C_o is the oxide capacitance per unit area, and V_{FB} is the flatband voltage.

Considering an n-MOSFET, neglecting the contribution of holes and assuming $\beta\psi \gg 1$, the electric field can be obtained from (1) following the conventional procedure of changing variables and integration [15,16]:

$$F = -\frac{d\psi}{dx} = -\sqrt{\frac{2kT n_i}{\epsilon_s}} \sqrt{e^{-\beta V} (e^{\beta\psi} - e^{\beta\psi_o})} \quad (4)$$

where $\psi_o \equiv \psi(x=0)$ is the potential extremum at the center of the channel.

Substituting (4) evaluated at the surface, with $\psi_s \equiv \psi(x=t_{Si}/2)$, into (3) yields:

$$V_{GS} - V_{FB} = \psi_s + \frac{\sqrt{2kT n_i \epsilon_s}}{C_o} \sqrt{e^{-\beta V} (e^{\beta\psi_s} - e^{\beta\psi_o})}. \quad (5)$$

The electron quasi-Fermi level gradient is in the y direction since the current flows only along the y direction. This justifies the approximation that assumes V to vary only along y and be constant in the x direction. Following the procedure proposed by Taur, (3) can be integrated again [4,5,7] to express the potential across the channel region as a function of x :

$$\psi(x) = \psi_o - \frac{2}{\beta} \ln \left\{ \cos \left[\sqrt{\frac{q^2 n_i}{2kT \epsilon_s}} e^{\frac{\beta(\psi_o - V)}{2}} x \right] \right\}. \quad (6)$$

Evaluating at the surface $x = t_{Si}/2$ and rearranging (6) yields

$$e^{\frac{\beta(\psi_o - \psi_s)}{2}} = \cos(\zeta). \quad (7)$$

where

$$\zeta = \sqrt{\frac{q^2 n_i}{2kT \epsilon_s}} e^{\beta(\psi_o - V)} \frac{t_{Si}}{2}. \quad (8)$$

The simultaneous solution of (5) and (7) allows to find the surface potential in terms of the terminal voltages V_{GS} and V . However, direct calculation requires numerical iteration and renders this approach computationally inefficient for circuit simulation compact model purposes.

III. ANALYTIC SOLUTION

Analyzing (5) we observe that, except for the exponential term with ψ_o , this equation is similar to the case of the single-gate bulk device, whose surface potential can be solved explicitly using the Lambert Function, as previously presented by us [8].

Following the same solution approach for the symmetric DG device, factoring the surface potential out of the radical in (5) yields

$$V_{GS} - V_{FB} = \psi_S + \frac{\sqrt{2kT n_i \epsilon_s}}{C_o} e^{\frac{\beta(\psi_S - V)}{2}} \sqrt{1 - e^{\beta(\psi_o - \psi_S)}}. \quad (9)$$

Substitution of (7) into the second radical of (9), and using the trigonometric identity $\sin^2(\zeta) + \cos^2(\zeta) \equiv 1$, yields the equation for the gate voltage that is to be solved in terms of the surface potential:

$$V_{GS} - V_{FB} = \psi_S + \frac{\sqrt{2kT n_i \epsilon_s}}{C_o} e^{\frac{\beta(\psi_S - V)}{2}} \sin(\zeta). \quad (10)$$

The above equation clearly has the form of Lambert's equation. Therefore solving for ψ_S finally yields the desired closed-form analytic solution for the surface potential of the undoped-body symmetric DG device as a function of the terminal voltages:

$$\psi_S = V_{GS} - V_{FB} - \frac{2}{\beta} W \left(\frac{\beta}{C_o} \sqrt{\frac{kT n_i \epsilon_s}{2}} e^{-\frac{\beta V}{2}} \sin(\zeta) e^{\frac{\beta(V_{GS} - V_{FB})}{2}} \right), \quad (11)$$

where W is the usual short-hand notation for the principal branch of the Lambert Function. Except for the term $\sin(\zeta)$ this expression is the same as that previously proposed for the undoped-body single-gate bulk device [8]. However, in this symmetric DG case we now require the additional knowledge of ζ , which depends on ψ_o , as indicated by (8).

IV. POTENTIAL EXTREMUM

In a symmetric DG MOSFET under equal bias on both gates the electric field vanishes at the center of the channel ($x = 0$), as indicated by (2). Therefore the channel potential reaches an extremum, $\psi(x=0) = \psi_o$, at that point.

Analyzing the phenomenological behavior of ψ_o , presented in Fig. 2, we observe that below threshold, while the semiconductor charge remains small, there is volume

inversion and the potential stays essentially flat ($\psi_S \approx \psi_o$) throughout the entire silicon film thickness, closely following the gate voltage everywhere (see also Fig. 3). As the gate voltage increases towards threshold the electron density becomes more and more significant. After threshold ψ_S continues to increase while ψ_o quickly departs from ψ_S until it saturates to a maximum value $\psi_{o\max}$ for higher gate voltages (see Fig. 3).

Furthermore, given that the argument ζ is restricted to between 0 and $\pi/2$, the maximum value that the potential extremum can reach at the center of the channel is given by

$$\psi_{o\max} = V + \frac{1}{\beta} \ln \left(\frac{2\pi^2 \epsilon_s kT}{q^2 n_i t_{si}^2} \right). \quad (12)$$

Therefore, it may be concluded that as gate voltage increases, ψ_o changes from linear behavior ($\psi_o \approx V_{GS} - V_{FB}$) below threshold, to saturated behavior ($\psi_o \approx \psi_{o\max}$) above threshold, as clearly illustrated in Fig. 3.

This behavior of ψ_o may be portrayed as a function of gate voltage by the use the following well known smoothing function, previously used to model drain voltage saturation behavior [17]:

$$\psi_o = U - \sqrt{U^2 - (V_{GS} - V_{FB})\psi_{o\max}}, \quad (13)$$

where

$$U = \frac{1}{2} [(V_{GS} - V_{FB}) + (1+r)\psi_{o\max}], \quad (14)$$

and r is the shoulder smoothing parameter which may be considered to be a fitting parameter or determined from its physical dependencies.

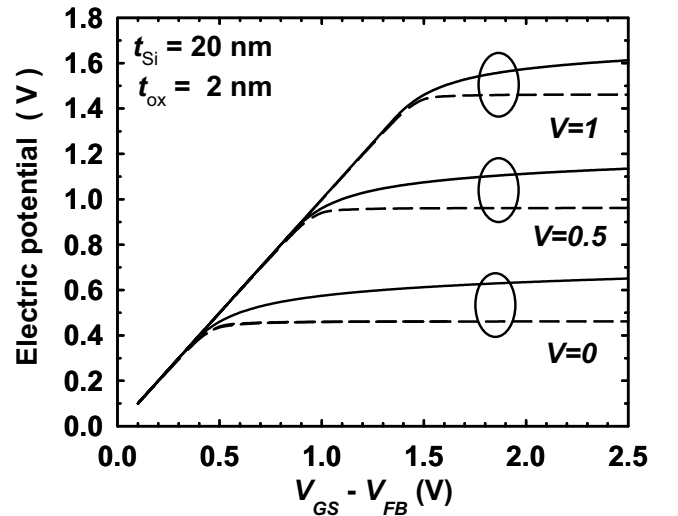


Fig. 3 Surface potential, ψ_S , (continuous lines) and potential extremum (at the center of the channel), ψ_0 , (broken lines) versus gate voltage.

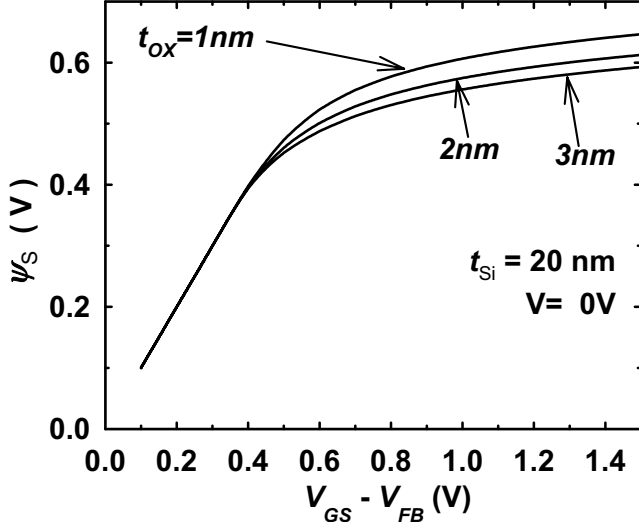


Fig. 4 Surface potential versus gate voltage for different gate oxide thicknesses.

In this case the smoothing parameter r is weakly dependent on t_{ox} , t_{Si} and V , and it may be represented by an empiric equation of the form

$$r = (At_{ox} + B) \left(\frac{C}{t_{Si}} + D \right) e^{-EV}, \quad (15)$$

with the values of $A=0.0267 \text{ nm}^{-1}$, $B=0.0270$, $C=0.4526 \text{ nm}$, $D=0.0650$, and $E=3.2823 \text{ V}^{-1}$ being appropriate for the typical device dimensions and operating ranges of interest.

Substituting (13) into (11), through (8), a closed form expression results for the undoped-body symmetric DG device surface potential as a function of the terminal voltages and the silicon film and gate oxide thicknesses.

Figure 3 presents the calculated potential at the center of the channel, ψ_0 , and the corresponding surface potential, ψ_S , versus gate voltage for three values of voltage along the channel. Figure 4 shows that the surface potential is affected by gate oxide thicknesses in the above threshold region, but it is independent of it below threshold.

IV. EXACT NUMERICAL SOLUTION

The following numerical computation procedure will be used to obtain an exact numerical solution for comparison purposes. This procedure could also be useful for modeling purposes, whenever an exact numerical solution of the problem is considered necessary.

For convenience sake, let us rename the cosine term in (7) as

$$\alpha_n = \cos(\zeta) \quad (16)$$

Recalling (7) and (8) and rearranging we may write:

$$f(\alpha_n) = \cos \left[\sqrt{\frac{q^2 n_i}{2kT \epsilon_s}} e^{\frac{\beta(\psi_S - V)}{2}} \frac{t_{Si}}{2} \alpha_n \right] - \alpha_n = 0 \quad (17)$$

where ψ_S is to be expressed in terms of α_n through (16) and (10). The solution for α_n is bounded by $0 < \alpha_n < 1$ and it can be obtained iteratively starting from an initial value of $\alpha_{n(i)}$, using a Newton-Raphson type procedure with

$$\alpha_{n(i+1)} = \alpha_{n(i)} - \frac{f(\alpha_{n(i)})}{f'(\alpha_{n(i)})}, \quad (18)$$

The convergence of the procedure is very fast and turns out to be computationally efficient.

Figure 5 presents the comparison of the surface and center-of-channel potentials versus gate voltage, as obtained analytically from (11) and by exact numerical calculation.

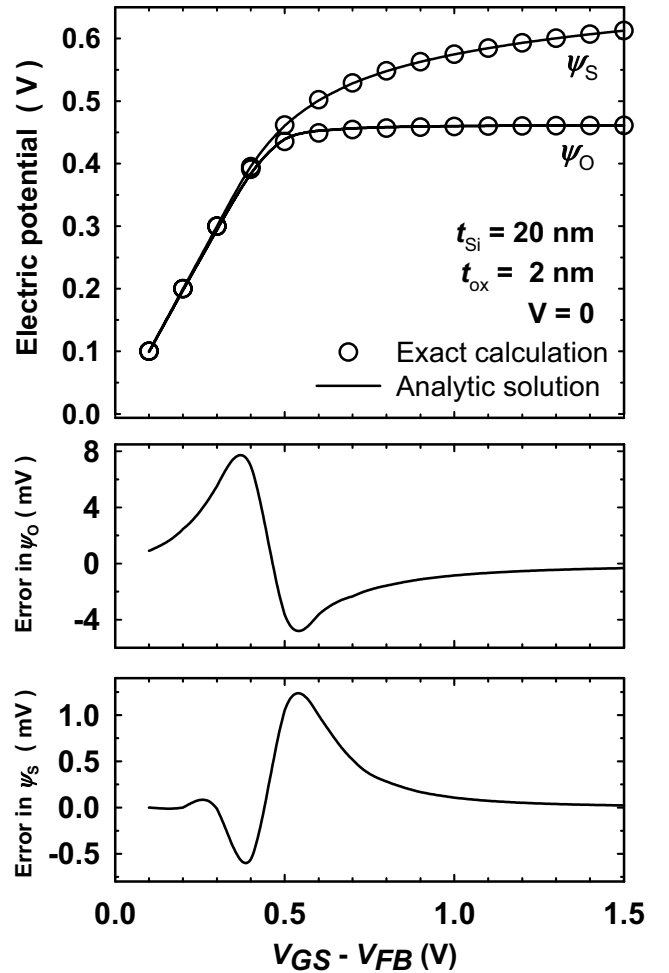


Fig. 5 Surface potential, ψ_S , and potential at the center of the channel, ψ_0 , versus gate voltage, as obtained analytically from (11) (continuous lines) and

by exact numerical calculation (symbols), together with the corresponding errors.

Notice that although ψ_0 is used, through ζ , to calculate ψ_S in (11), the error in ψ_S turns out to be considerably smaller than that in ψ_0 , clearly suggesting that ψ_0 modeling needs not be too strict.

V. CHARGE MODELING

Since for an undoped body DG MOSFET the carrier charge per unit area Q_I induced in the channel represents the total charge in the semiconductor, we can calculate Q_I directly from (11) as

$$Q_I = 2C_o [(V_{GS} - V_{FB}) - \psi_S] \quad (19)$$

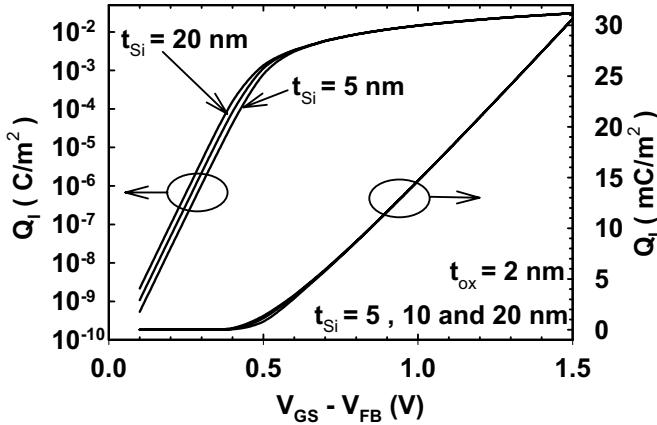


Fig. 6 Carrier charge per unit area induced in the channel as a function of gate voltage for three silicon film thicknesses, assuming zero drain-to-source voltage.

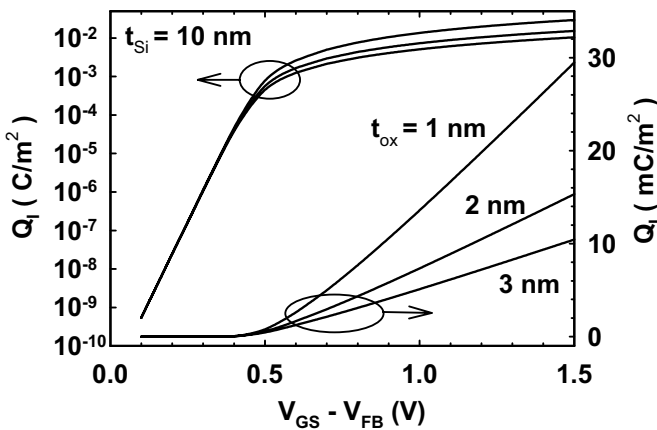


Fig. 7 Carrier charge per unit area induced in the channel as a function of gate voltage for three oxide thicknesses, assuming zero drain-to-source voltage.

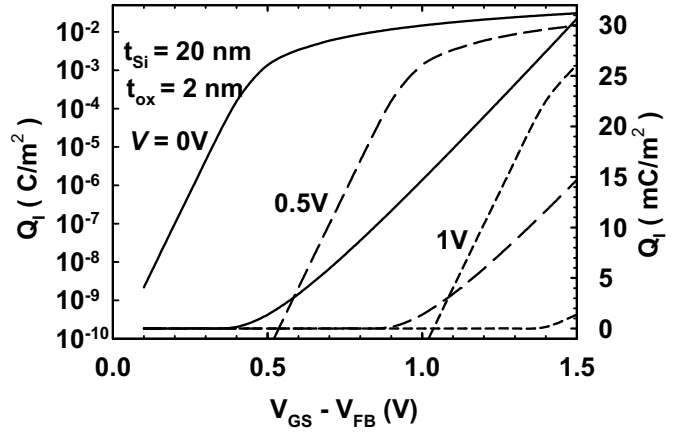


Fig. 8 Carrier charge per unit area induced in the channel as a function of gate voltage for three values of channel voltage.

Figures 6 to 8 present the carrier charge per unit area induced in the channel versus the applied gate voltage, for various silicon film thicknesses, gate oxide thicknesses, and channel voltages, as calculated using (19). The charge sub-threshold slope, S , measured as the inverse of the semi-logarithmic charge-gate voltage characteristics slope, as expected has a value very close to the ideal value of 60 mV per decade of charge change. This sub-threshold slope is not affected by gate oxide thickness, as it is in the case of conventional doped-body devices. We notice that the silicon thickness affects the carrier charge below threshold but has little effect above threshold. This is consistent with the fact that below threshold there is volume inversion and the charge is essentially proportional to silicon film thickness for a given gate voltage bias. Figure 6 also indicates that the on-off ratio increases as the silicon film thickness decreases. Conversely, the carrier charge per unit area induced in the channel in the above-threshold region is inversely proportional to the oxide thickness, as clearly illustrated in Fig. 7.

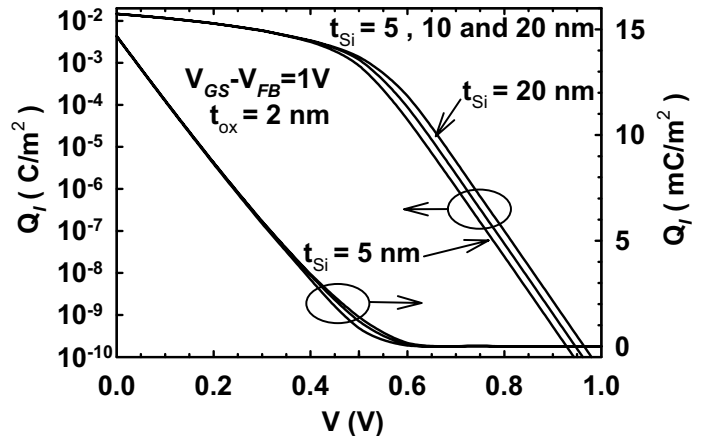


Fig. 9 Carrier charge per unit area induced in the channel as a function of channel voltage for three silicon film thicknesses, at a given gate voltage.

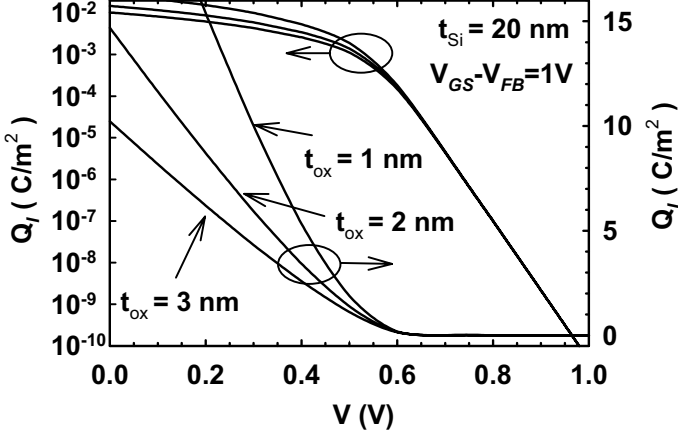


Fig. 10 Carrier charge per unit area induced in the channel as a function of channel voltage for three gate oxide thicknesses, at a given gate voltage

Figures 9 and 10 show the variation of the carrier charge per unit area induced in the channel as a function of the channel voltage, for various silicon film thicknesses and gate oxide thicknesses, at a given gate voltage, as calculated from (19) with the surface potential given by (11).

VI. CONTINUOUS ANALYTIC CURRENT MODEL

Considering that the drain current may be represented by the addition of its diffusion and drift components, a recently proposed charge-based drain current formulation is [12]:

$$I_{DS} = \frac{W}{L} \mu_{eff} \left[\frac{Q_{IS}^2 - Q_{ID}^2}{4C_o} + \frac{1}{\beta} (Q_{IS} - Q_{ID}) \right], \quad (20)$$

where Q_{IS} and Q_{ID} are the total carrier charges per unit area evaluated at the source and drain, respectively. We assume a long channel device neglecting small dimensional effects, which may be included later into the current equation. The modeled drain current turns out to be continuous from below to above threshold, which results in continuity for higher derivatives.

Figure 11 presents the drain current-gate voltage transfer characteristics calculated using (20) with a constant effective mobility of $300\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and other parameters as indicated in the figure. Notice that the maximum error occurs around the threshold transition point. Figure 12 presents the analytically and numerically calculated drain current-drain voltage output characteristics for various values of gate voltage. It is worth observing that the relative error decreases as the gate voltage increases.

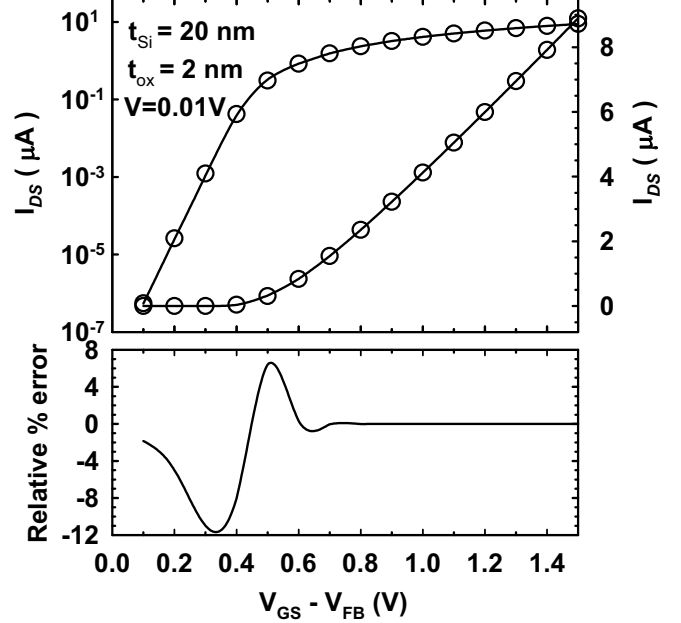


Fig. 11 Comparison of the drain current-gate voltage transfer characteristics as calculated analytically from (11) (continuous line) and from exact numerical calculations (symbols).

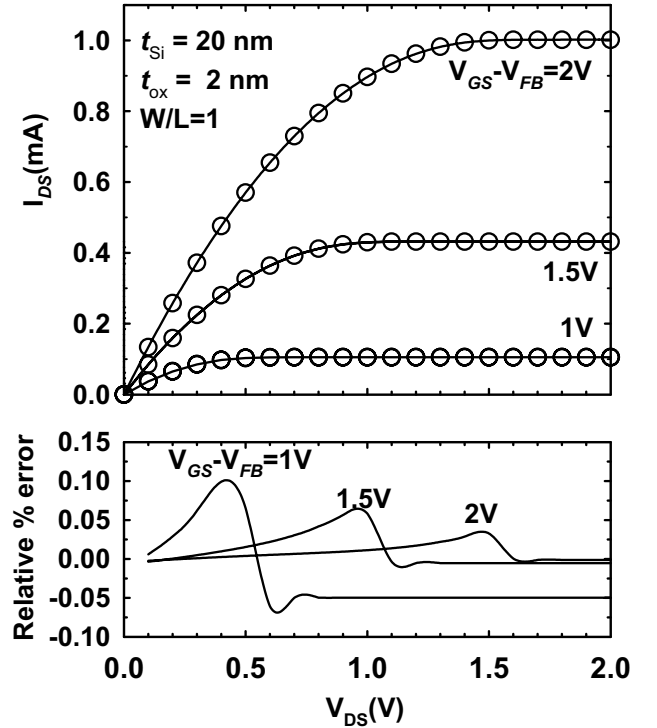


Fig. 12 Comparison of the drain current-drain voltage output characteristics as calculated analytically from (11) (continuous line) and from exact numerical calculations (symbols), for three values of gate voltage.

VII. CONCLUSIONS

A computationally efficient and physically meaningful surface-potential compact model of the undoped-body

symmetric DG MOSFETs has been presented. The model is an accurate analytic solution of the surface potential as an explicit function of the gate voltage, which was developed based on our previous solution for undoped bulk SG MOSFET using Lambert W functions. The solution, given by (11), is continuously valid for all regions of operation of this particular kind of device from subthreshold to strong inversion.

The error range generated by this solution seems to be reasonably small for typical device dimensions and bias conditions. This analytic solution may be used directly in surface potential-based current models by evaluating at the drain and source ends of the channel. Alternatively, the total inversion charge at the drain and source ends is calculated from the potential model and then introduced in a recently proposed charge-based drain current model [12]. Additionally we have presented a quickly converging iteration procedure, used here to get the exact solution for comparison purposes, but which may be used also to efficiently calculate an exact numerical solution whenever greater precision is required.

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