PERGAMON

Microelectronics Reliability 42 (2002) 343–347

MICROELECTRONICS RELIABILITY

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Influence of polysilicon-gate depletion on the subthreshold behavior of submicron MOSFETs

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Received 11 July 2001; received in revised form 27 November 2001

Abstract

Ion implantation, followed by annealing process, often leads to nonuniform doping and considerable depletion effect in the polysilicon gate of submicron MOS devices. Such an effect can alter notably the subthreshold characteristics and invalidate the conventional subthreshold current model. This paper studies the polysilicon-gate depletion effects on the subthreshold behavior based on results obtained from two-dimensional device simulation. An empirical expression is also suggested to describe the subthreshold current including the depletion effect. © 2002 Elsevier Science Ltd. All rights reserved.

1. Introduction

Ion implantation, followed by annealing process, is often used to form the drain and source regions, and at the same time provides the doping source for the polysilicon gate of MOSFETs. The scaling of MOSFET has decreased the gate oxide thickness and increased the substrate doping density. To prevent the doping in polysilicon from entering the thin oxide, implant dose with a relatively low energy is preferred. This nonetheless gives rise to an insufficient doping in the polysilicon gate near the oxide and thus a considerable polysilicon-gate depletion effect, which degrades MOSFET performance. Many publications [1–9] have analyzed the effect of polysilicon-gate depletion on the threshold voltage and on the capacitance. These analyses have been focused on the MOSFET characteristics in strong inversion. Moreover, it has been a common practice to assume that the doping density in the polysilicon gate is uniform. This assumption is questionable as the ion-implanted doping density, even after annealing, in the polysilicon gate is position dependent.

In this paper, we study the effect of polysilicon-gate depletion on the subthreshold (i.e., weak inversion) behavior of submicron MOSFETs. Our analysis will remove the conventional assumption of uniform doping in the polysilicon gate and will be based on results obtained from the two-dimensional process and device simulators ATHENA and ATLAS [10]. Various implant energies will be considered, and their impacts on the subthreshold current of MOSFETs will be discussed.

2. Device structure used in atlas

Several n-channel MOSFETs were simulated under different ion implantation conditions in the polysilicon

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PII: S0026-2714(01)00259-1

gate. All simulated devices had a mask channel length of 0.2 μm, drain/source contact width of 0.1 μm, separation of 0.2 μm between contacts and polysilicon gate, polysilicon-gate thickness of 0.2 μm, substrate doping concentration of 5×10^{17} cm^{-3}, drain/source junction depth of 75 nm with a lateral extent of 53 nm (70% of their vertical extent) with respect to the spacer, and gate oxide thickness of 6 nm (i.e., the oxide capacitance is 5.75×10^{-7} F/cm^2).

Given the implant dose, implant energy, and annealing condition (i.e., time and temperature), ATHENA can yield the doping profile in the polysilicon gate. This, together with other device make-ups specified, allows ATLAS to generate the current–voltage characteristics of MOSFET by solving numerically the Poisson equation, electron and hole continuity equations, and electron and hole current equations.

Calibration of ATHENA and ATLAS is an important step in generating accurate and reliable simulation results. To this end, we have calibrated ATHENA and ATLAS against experimental data measured from a MOSFET with a channel length of 0.5 μm, poly implant dose of 10^{15} cm^{-2}, poly implant energy of 30 KeV, and substrate doping density of 5×10^{17} cm^{-3}. The resulting simulated and measured current–voltage characteristics are compared in Fig. 1, and reasonable agreement is obtained.

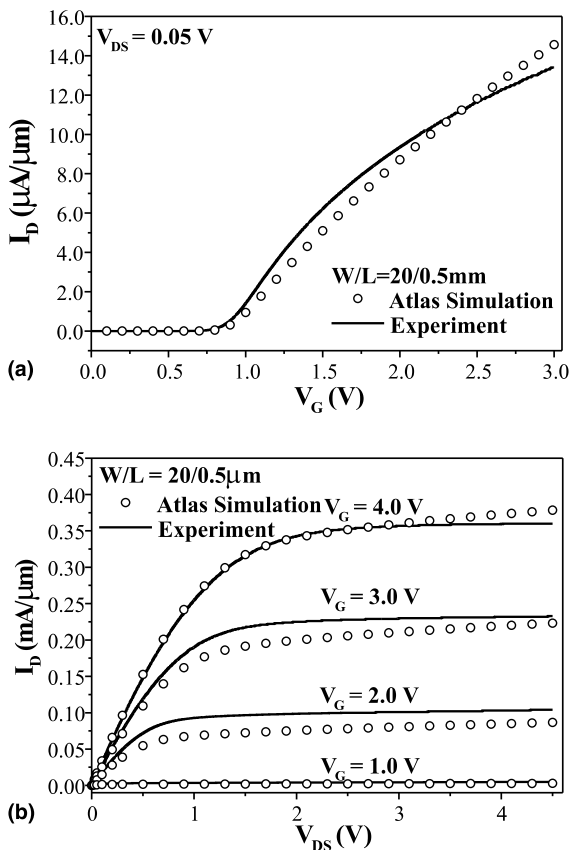

Fig. 1. Comparison of simulated and measured (a) drain current versus gate voltage and (b) drain current versus drain voltage characteristics of an *n*-channel MOSFET having a channel length of 0.5 μm and channel width of 20 μm.

3. Simulation results and discussions

Fig. 2 illustrates the simulated doping concentration in the polysilicon gate versus the distance for a Phosphorous dose of 10^{15} cm^{-2} and four different implant energies (i.e., 10, 20, 30, and 40 KeV), followed by an annealing condition of 850 °C and 10 min. The dose, energies, and annealing are those typically used in the 0.2 μm CMOS technology. The case of a uniform doping in the polysilicon gate is also included for comparison. We see in this figure that the lower the energy, the lower the doping density in the region near the oxide (i.e., $x = 0.2$ μm is the polysilicon–oxide interface), and thus the more significant the polysilicon depletion effect. In other words, the doping in polysilicon becomes more uniform if the implant energy is increased. Another observation is that the peak density increases slightly with increasing implant energy.

Fig. 3 presents the subthreshold drain current I_D versus gate voltage V_G for the different ion implant cases considered. Note that because of the nature of two-dimensional simulation, the unit of the current is A/μm, where μm being the third dimension. A small applied drain voltage $V_{DS} = 50$ mV was used to ensure the MOSFETs operated in the linear region. Comparing the results of the uniform doping and the nonuniform doping from ion implant and annealing, it is evident that

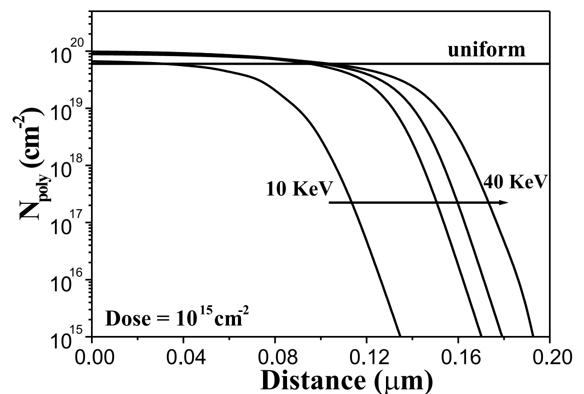

Fig. 2. Doping concentration in the polysilicon gate versus the distance for an Phosphorous dose of 10^{15} cm^{-2} and four different energies (10, 20, 30 and 40 KeV). An annealing of 850 °C and 10 min was performed after the implantation.

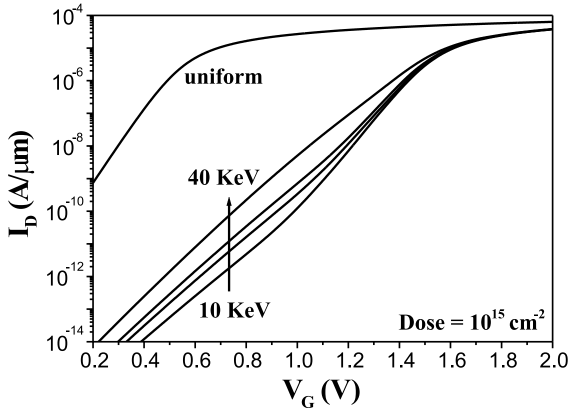

Fig. 3. Simulated subthreshlod drain current versus gate voltage characteristics for the different ion implant conditions considered.

the polysilicon-gate depletion effect increases the threshold voltage and decreases the drain current, particularly in the subthreshold region. Moreover, the characteristics of the subthreshold current are affected by the polysilicon-gate depletion. For the case of high implant energies (i.e., 40 KeV), which is close to the uniform doping, the conventional single-exponential I_D–V_G dependence is observed. However, as the implant energy is reduced, and thus the importance of depletion effect is increased, the subthreshold current deviates from the single-exponential function and exhibits a trend of two different slopes on the logarithm scale, as shown clearly in the case of 10 KeV in Fig. 3.

To aid the discussions, let us examine the conventional subthreshold current model, which has the following form [11–13]:

$$I_D = \frac{W}{L} I_M \exp\left(\frac{V_G - V_M}{nV_{th}}\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_{th}}\right)\right) \quad (1)$$

where I_D is the drain current, W is the channel width, L is the channel length, V_{th} is the thermal voltage, I_M and V_M are the constant parameters for current and voltage, respectively, and n is the ideality factor. Eq. (1) can be rewritten as

$$I_D = I_X \exp\left(\frac{V_G}{nV_{th}}\right) \quad (2)$$

where

$$I_X \equiv \frac{W}{L} I_M \exp\left(\frac{-V_M}{nV_{th}}\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_{th}}\right)\right) \quad (3)$$

is a constant if V_{DS} is fixed. Then, taking the natural logarithm on both sides of Eq. (2) and a derivative with respect to V_G, we obtain

$$n = \frac{1}{V_{th}} \frac{\ln(10)}{\frac{d\ln(I_D)}{dV_G}} \quad (4)$$

Ideally, $n = 1$ at room temperature. As will be shown below, however, n is normally larger than unity.

The preceding analysis has suggested that the conventional subthreshold current model would fail when the polysilicon-gate depletion effect becomes significant (i.e., cases of low implant energies). We propose the following empirical model to describe the subthreshold current having two different slopes results from the polysilicon-gate depletion effect:

$$I_D = I_{D1} + I_{D2} \quad (5)$$

where

$$I_{D1} = I_{X1} \exp\left(\frac{V_G}{n_1 V_{th}}\right) \quad (6)$$

$$I_{D2} = I_{X2} \exp\left(\frac{V_G}{n_2 V_{th}}\right) \quad (7)$$

and n_2, n_1, I_{X2}, and I_{X1} are empirical parameters. This model is analogous to the parallel two-exponential diode model [13]. Each term in Eqs. (5)–(7) describes the drain current function in a region in which it dominates; $I_{D2} \gg I_{D1}$ for low voltages and $I_{D1} \gg I_{D2}$ for high voltages. Then, from the I–V characteristics shown in Fig. 3, the following relationship should be satisfied: $n_2 \gg n_1$ and $I_{X2} \gg I_{X1}$. Therefore, the parameters n_2 and I_{X2} are obtained by using $I_D \approx I_{D2}$ for low voltages, and parameters n_1 and I_{X1} are determined by using $I_D \approx I_{D1}$ for higher voltages.

Fig. 4 compares the subthreshold drain currents obtained from the empirical model (dashed lines) and from device simulation (closed circles) for an implant dose of

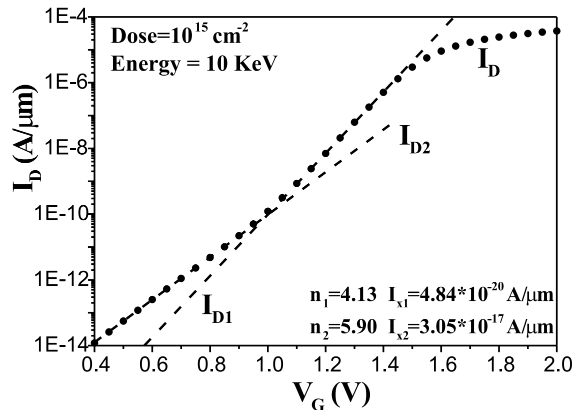

Fig. 4. Subthreshold drain current versus gate voltage V_G obtained from the empirical model (– – –) and from simulation results (●) for the case of an implant dose of 10^{15} cm^{-2} and implant energy of 10 KeV.

10^{15} cm^{-2} and energy of 10 KeV. For this particular case, the polysilicon-gate depletion effect is not negligible, and the subthreshold behavior deviates considerably from the single-exponential function described by the conventional model. By fitting the empirical model with simulation results, $n_2 = 5.9$ and $n_1 = 4.13$ are obtained, and $I_{X2} = 4.84 \times 10^{-20}$ and $I_{X1} = 3.05 \times 10^{-17}$ A/μm are determined by extrapolating the straight lines of I_{D1} and I_{D2} to the vertical axis. Clearly, the empirical model agrees very well with the simulation results in the region of weak inversion.

We now examine the physics underlying the two different ideality factors associated with the subthreshold current for the case of low implant energy (i.e., hereafter called nonuniform case). Fig. 5(a) and (b) shows the simulated electrostatic potentials versus the vertical position (i.e., from polysilicon gate to silicon) taken at the middle of the channel for the uniform and nonuniform doping cases and for two different gate bias regions. Because of the two different slopes in two different gate bias regions, we consider the bias region of $V_G = 0.4$ and 0.5 V where the ideality factor is n_2 (Fig. 5(a)) as well as the bias region of $V_G = 1.0$ and 1.1 V where the ideality factor is n_1 (Fig. 5(b)). It is shown that, due to the depletion effect, the electrostatic potential ψ in the nonuniform case is a strong function of position, whereas ψ for the uniform case is almost a constant in the polysilicon. At the Si–SiO_2 interface, for the nonuniform doping case, we found that the potential difference $\Delta\psi$ is 17 mV when V_G increasing from 0.4 to 0.5 V. This value is noticeably smaller than $\Delta\psi$ of 39 mV when V_G increasing from 1.0 to 1.1 V. Since the inversion charge in silicon, and thus the drain current, is a function of the electrostatic potential at the interface, such a difference in $\Delta\psi$ explains the two ideality factors seen in the subthreshold current when the polysilicon-gate depletion effect is significant. For the uniform doping case, $\Delta\psi$ versus ΔV_G is the same throughout the subthreshold region, and thus a single ideality factor is observed.

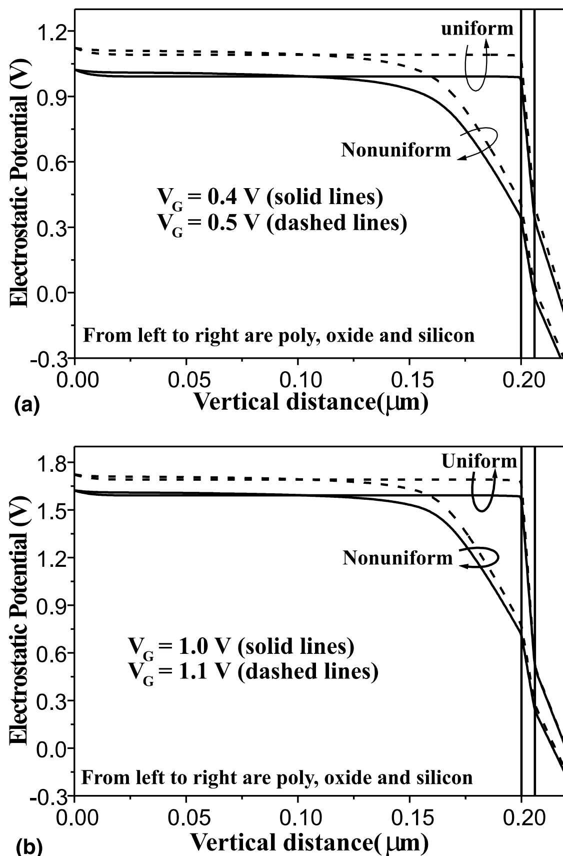

Fig. 5. Simulated electrostatic potentials versus vertical position (from polysilicon to silicon) taken at the middle of channel for the uniform and nonuniform (i.e., energy of 10 KeV) doping cases and for the gate bias regions of (a) 0.4–0.5 V, and (b) 1.0–1.1 V.

4. Conclusion

A two-dimensional numerical analysis has been presented to investigate the effect of polysilicon-gate depletion on the subthreshold behavior of submicron MOSFETs. In our study, the conventionally used assumption of uniform doping in the polysilicon gate was removed, and practical doping profiles resulted from various ion implantation conditions were considered. It was shown that for the cases of high implant energies, the MOSFET behaves similarly as the uniform doping case. But the conventional subthreshold model failed for the cases of low implant energies where the polysilicon-gate depletion effect is significant. An empirical model was also developed, which described successfully the abnormal subthreshold drain current observed in 0.2-μm MOS devices. The double-slope subthreshold current model developed can be utilized as a tool to characterize the effect of polysilicon depletion on the dc performance of MOSFETs under the subthreshold operation.

Acknowledgements

This work was supported by "Consejo Nacional de Investigaciones Científicas y Tecnologicas" through grant S1-98000567.

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