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Microelectronics Reliability 39 (1999) 1173–1184

MICROELECTRONICS RELIABILITY

www.elsevier.com/locate/microrel

Introductory invited paper

On the extraction of the source and drain series resistances of MOSFETs

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Received 20 February 1999

Abstract

This article reviews and scrutinizes various proposed methods to extract the individual values of drain and source resistances (R_D and R_S) of MOSFETs, which are important device parameters for modeling and circuit simulation. In general, these methods contain three basic steps: (1) the extraction of the total drain and source resistance ($R_D + R_S$); (2) the extraction of the difference between the drain and the source resistances ($R_D - R_S$); and (3) the calculation of R_D and R_S from the knowledge of ($R_D + R_S$) and ($R_D - R_S$). These methods are tested and compared in the environments of circuit simulator, device simulation and measurements.

1. Introduction

The drain and source parasitic resistances, R_D and R_S, of a MOSFET can be modeled by considering the intrinsic device with R_D and R_S connected in series with its intrinsic drain and source, respectively, as shown in Fig. 1. If the current that flows through the device channel is assumed to be the same as that flows through the drain and source series resistances, then the MOSFET's intrinsic gate-source voltage (V_{GS}), drain-source voltage (V_{DS}), and body-source voltage (V_{BS}) can be defined in terms of the drain current (I_d) and the extrinsic voltage counterparts V_{gs}, V_{ds}, and V_{bs} as

$$V_{GS} = V_{gs} - I_d R_S, \tag{1}$$

$$V_{DS} = V_{ds} - I_d(R_S + R_D), \tag{2}$$

$$V_{BS} = V_{bs} - I_d R_S. \tag{3}$$

Therefore, the extraction of the intrinsic device's parameters from experimental data requires either the knowledge of R_S and R_D, or the availability of a method capable of performing the extraction of the intrinsic model parameters independently of R_S and R_D [1–8].

The extraction of the total drain and source resistance ($R_D + R_S$) will first be covered in this article. Next, we will discuss the extraction of the difference between the two resistances ($R_D - R_S$), based on the physical insight provided by device simulation. The knowledge of these two quantities will allow the determination of the individual values of R_D and R_S.

2. Extraction of total drain and source series resistance

The extraction of the individual values of the source

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0026-2714/99/$ - see front matter
PII: S0026-2714(99)00028-1

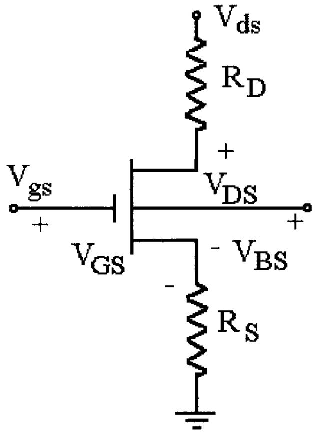

Fig. 1. MOSFET equivalent circuit with drain and source series resistances.

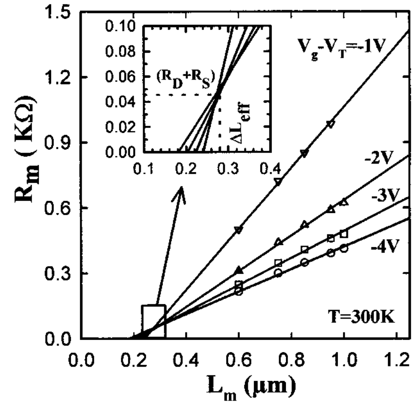

Fig. 2. Total measured channel resistance versus mask channel for various gate bias. The unique intersection of all the straight lines yields to the total drain and source resistance.

$$R_m = \frac{V_{ds}}{I_d} \approx (R_D + R_S) + \frac{(L_m - \Delta L_{eff})}{W\mu C_o(V_{gs} - V_T)} \quad (6)$$

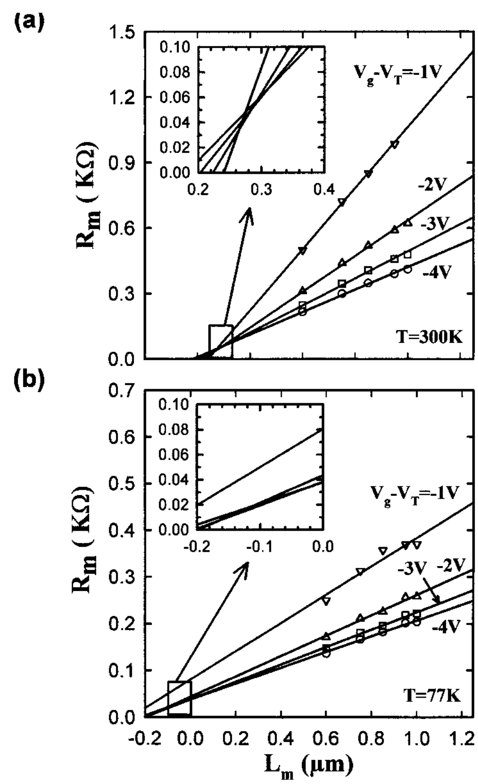

Fig. 3. Total measured channel resistance versus mask channel length for various gate voltages at (a) 300 K and (b) 77 K. The symbols are the measured data and the lines are the fittings to data using straight lines. Terada's method fails for 77 K because there is not a unique intersection of all the straight lines.

and drain series resistances require either the knowledge of their sum $(R_D + R_S)$ and difference $(R_D - R_S)$, or the ability to extract the two parameters separately. In this section, we will deal with the extraction of $(R_D + R_S)$. The extraction of $(R_D - R_S)$ will be presented in the Section 3.

The most widely used method to extract the total drain and source series resistance $(R_D + R_S)$ was presented independently by Terada and Muta [9] and by Chern et al. [10] almost 20 years ago. Several other methods [11–24] have been developed recently.

2.1. Terada–Muta or Chern et al. method

The derivation of this method was based on a simple current–voltage relationship for MOSFET. Fig. 1 shows the MOSFET equivalent circuit including the drain and source series resistances, and with the source terminal grounded. The drain current I_d in the linear region can be expressed as [8]

$$I_d = \frac{W}{L_{eff}} \mu C_o (V_{GS} - V_T) V_{DS} \quad (4)$$

where W is the channel width, L_{eff} is the effective channel, C_o is the oxide capacitance per unit area, μ is the effective free-carrier mobility, and V_T is the threshold voltage. Combining Eqs. (4) and (2), the total channel resistance, R_m, can be expressed by

$$R_m = \frac{V_{ds}}{I_d} = (R_D + R_S) + \frac{(L_m - \Delta L_{eff})}{\mu C_o W (V_{GS} - V_T)} \quad (5)$$

where L_m is the mask channel length and $\Delta L_{eff} \equiv (L_m - L_{eff})$. For the linear region under study, $(V_{gs} - V_T)$ is much larger than $I_d R_{DS}$, and $V_{gs} \approx V_{GS}$. This results in

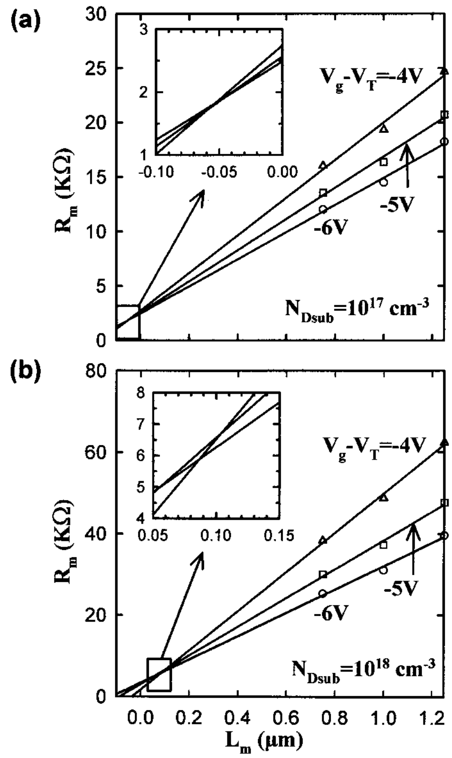

Fig. 4. Simulated total channel resistance versus mask channel length for two different MOSFETs with: (a) $N_A^+ = 10^{20}$ cm^{-3} and $N_{Dsub} = 1018$ cm^{-3}; and (b) $N_A^+ = 1020$ cm^{-3} and $N_{Dsub} = 1017$ cm^{-3}. Terada's method fails for case (b) because there is not a unique intersection of all the straight lines.

According to Eq. (6), plotting R_m versus L_m for different values of $(V_{gs} - V_T)$, having previously extracted V_T, should produce a family of straight lines, all intersecting at one point of which the abscissa yields ΔL_{eff} and the ordinate yields $(R_D + R_S)$ [9]. This plot, together with the intersection of the straight lines, is illustrated in Fig. 2. Note that the Terada–Muta method requires a set of several MOS devices having different L_m but otherwise identical device make-up. It is important to point out that the threshold voltage should be extracted from other methods and that the value of V_T is a function of L_m.

Although widely used, the Terada–Muta method has been found to fail in yielding accurate values of L_{eff} for MOSFETs operating at liquid nitrogen temperature [17,25]. An example of this failure is illustrated in Fig. 3(a) and (b), which show the R_m versus L_m plots of p-channel devices at temperatures of 300 and 77 K, respectively. At 300 K, the unique intersection of the straight lines yields $\Delta L_{eff} \approx 0.3$ μm on the x-axis and $(R_{DS} + R_{DS}) \approx 60$ Ω on the y-axis. On the other hand, the analogous procedure at 77 K does not yields a unique intersection of the straight lines, and even if the intersection of three of lines is used, a negative value of ΔL_{eff} is obtained, which is possible for the lightly-doped drain (LDD) MOSFET but is physically unsound for the conventional MOSFET under consideration [26].

The Terada method may also fail at room temperature under certain conditions. Recent two-dimensional device simulations [26], illustrated in Fig. 4(a) and (b) for MOSFETs with two different substrate doping concentrations N_{Dsub}, have shown that such a method fails for MOSFETs having a relatively high doping concentration in the substrate. The simulated p-channel LDD MOSFETs had different N_{Dsub}, but the same heavily-doped source and drain p-type Gaussian profile with a peak doping concentration of N_A^+. In Fig. 4(a), $N_A^+ = 10^{20}$ cm^{-3} and $N_{Dsub} = 10^{17}$ cm^{-3} are considered, and a macroscopically unique intersection of the straight lines is obtained, which yields $R_{DS} = 1.8$ kΩ and $\Delta L_{eff} = -0.05$ μm. When N_{Dsub} is increased to 10^{18} cm^{-3}, however, more than one intersection exists (see Fig. 4(b)), and the precise value of ΔL_{eff} is not clear. As a result, it can be concluded that the Terada method becomes questionable for MOSFETs having a relatively low N_A^+ to N_{Dsub} ratio.

The failure of the Terada's method can be attributed to the following questionable assumptions implicitly used in developing the method: (1) the drain and source series resistances are independent of the gate bias; (2) the threshold voltage used in the method does not account for the effects of the series resistances; (3) $V_{gs} \approx V_{GS}$; and (4) the free-carrier velocity saturation effect in the channel is negligible.

Recently, Terada and co-workers presented an improved extraction method [27], which proposed that ΔL_{eff} and R_{DS} extracted using their original method can be a function of the gate voltage due to the fact that the R_m versus L_m plot possesses several intersections of the straight lines. From these different intersections, a statistical approach is then used in their new method to determine the correct and unique ΔL_{eff} and R_{DS} based on the concept that the most accurate ΔL_{eff} and R_{DS} give rise to the least dependence of these two parameters on the gate bias.

2.2. Recent methods

Recently many recent methods have been proposed to extract the total drain and source resistance, using either a single device or a set of devices with different channel lengths [15–20]. For example, a method [21] has been proposed to use the nonlinear optimization, together with an iterative linear regression procedure, to extract the threshold voltage, the effective geometry, and the total parasitic series resistance. The method uses one set of data obtained in the linear region of several MOSFETs having different geometries.

Methods that only require a single device to extract $(R_D + R_S)$ are always preferable when the goal is to extract the individual source and drain resistances. A method has been developed based on using a single device [22,23]. It determines the source or drain series resistance either from the device dc characteristics at V_{ds} approaching zero, or from the device frequency response subject to an ac signal with small magnitude and low frequency [23]. However, such a procedure assumes symmetrical drain and source configurations, and therefore becomes questionable when $R_S \neq R_D$.

The extrinsic drain conductance $(g_d = \partial I_d/\partial V_{ds})$, gate transconductance $(g_m = \partial I_d/\partial V_{gs})$, and body transconductance $(g_b = \partial I_d/\partial V_{bs})$ are also useful to extract the drain and source resistances. Simple circuit theory relates these extrinsic parameters to their intrinsic counterparts (i.e., g_{m0},g_{d0},g_{b0}). Assuming that the drain current (I_d) passing through R_S, R_D, and the intrinsic MOSFET channel is the same, and considering R_S and R_D are gate-voltage dependent and R_D is also drain-voltage dependent, yields [28]:

$$\frac{g_m}{g_{m0}} = \frac{1 - \frac{(g_{m0}+g_{b0})}{g_{m0}} I_d \frac{\partial R_S}{\partial V_{gs}} - \frac{g_{d0}}{g_{m0}} I_d \frac{\partial (R_S + R_D)}{\partial V_{gs}}}{1 + (g_{m0}+g_{b0})R_S + g_{d0}(R_S+R_D)}, \tag{7}$$

$$\frac{g_d}{g_{d0}} = \frac{1 - I_d(\partial R_D/\partial V_{ds})}{1 + (g_{m0}+g_{b0})R_S + g_{d0}(R_S+R_D)} \tag{8}$$

and

$$\frac{g_b}{g_{b0}} = \frac{1 - \frac{(g_{m0}+g_{b0})}{g_{b0}} I_d \frac{\partial R_S}{\partial V_{bs}} - \frac{g_{d0}}{g_{b0}} I_d \frac{\partial (R_S + R_D)}{\partial V_{bs}}}{1 + (g_{m0}+g_{b0})R_S + g_{d0}(R_S+R_D)}. \tag{9}$$

For the particular case in which the voltage dependencies of R_S and R_D are negligible, Eqs. (7)–(9) yield to

$$\frac{g_m}{g_{m0}} \approx \frac{g_d}{g_{d0}} \approx \frac{g_b}{g_{b0}} \approx \frac{1}{1 + (g_{m0}+g_{b0})R_S + g_{d0}(R_S+R_D)}. \tag{10}$$

For long channel devices, operating in the linear region at a very small drain-to-source voltage, g_{m0} and g_{d0} can be neglected in the saturation region. However, these terms are important and cannot be omitted for short channel devices.

Using Eq. (10) and assuming that R_S and R_D are bias independent, the ratio of the drain conductance to the gate transconductance is [29]

$$\frac{g_d}{g_m} \approx \frac{g_{d0}}{g_{m0}} \approx \frac{V_{GS} - V_T}{V_{DS}} \tag{11}$$

where V_T is the threshold voltage. Replacing the intrinsic voltages by their extrinsic counterparts, together with Eqs. (1) and (2), yields

$$V_{gs} - \frac{g_d}{g_m}\left[V_{ds} - I_d(R_D - R_S)\right] = I_d\left(1 - \frac{2g_d}{g_m}\right)R_S + V_T. \tag{12}$$

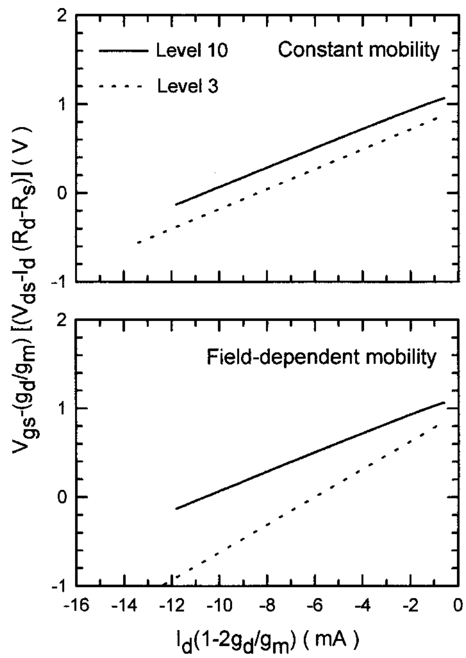

Fig. 5. Simulations with AIM-SPICE showing the characteristics of Eq. (12) with different MOSFET models (i.e., level-10 and level-3 models) and different free-carrier mobility models.

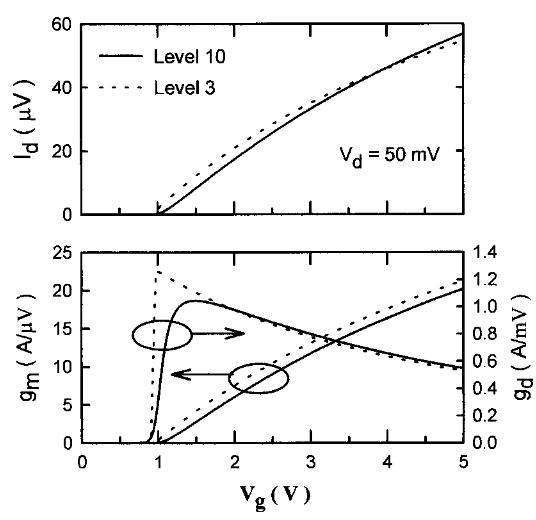

Fig. 6. Simulations with AIM-SPICE showing I_d, g_m, and g_d versus V_g with different MOSFET models (i.e., level-10 and level-3 models).

The plot of the left-hand side of Eq. (12) versus the multiplicand of R_S on the right-hand side of Eq. (12), at various bias points, should produce a straight line with a slope equal to R_S. In addition, the intercept of the line at the voltage axis gives the value of V_T. The value of R_D can then be found, provided the value of $(R_D - R_S)$ is known.

Fig. 5 illustrates this method. It shows the results of the left-hand side of Eq. (12) versus the first term on the right-hand side of Eq. (12) simulated using AIM-SPICE simulator with level-10 and level-3 MOSFET models. In addition to the two different models, both the constant and field-dependent free-carrier mobilities were considered. As mentioned earlier, the slope of the line gives R_S and the intercept of the line at the x-axis gives V_T. It is apparent that the level-10 results are independent of the type of mobility used and thus are more reliable than the level-3 counterpart. Fig. 6 shows the simulated I_d, g_m, and g_d versus V_g characteristics. Again, a notable discrepancy is found between the results simulated using level-10 and level-3 MOSFET models.

2.3. Total drain and source resistance bias dependencies

Two-dimensional device simulations revealed that the drain resistance increases with decreasing gate voltage and/or increasing drain voltage [30]. In general, both the source and drain series resistances, R_S and R_D, are gate-voltage dependent, and the drain resistance R_D is drain- voltage dependent as well. The conventional Terada's method [9] has been used to study the dependence of the total source and drain resistance $(R_D + R_S)$ on gate voltage. Using this technique, Hu et al. [30] found that the gate-bias dependent total series resistance of MOSFETs can be expressed in the form

$$(R_S + R_D) = K - C\log\left(V_{gs} - V_T\right) \tag{13}$$

where K and C are constants. This idea of using Terada's method to obtain the bias dependencies of the series resistance is questionable because Terada's method implicitly assumed that the series resistances are bias independent.

The dependence of the source and drain resistances on gate-voltage and the dependence of the drain resistance on drain-voltage can also be determined from a single device without utilizing any particular model for the MOSFET [28]. Based on this approach, the drain-voltage dependence of the drain resistance (i.e., $\partial R_D/\partial V_{ds}$) is found by first adding an external resistor R_{ext} in series with the drain terminal. The reciprocal of the drain conductance, given by Eq. (8), is then plotted for various V_{ds} and at a constant V_{gs}, as a function of the externally added drain resistor. Calculating the slopes of the resulting straight lines permits the determination of $\partial R_D/\partial V_{ds}$, since according to Eq. (8) the slope is

$$\frac{\partial g_d^{-1}}{\partial R_{ext}} = \frac{1}{1 - I_d(\partial R_D/\partial V_{ds})}. \tag{14}$$

The gate-voltage dependence of the total drain and source resistances (i.e., $\partial(R_D + R_S)/\partial V_{gs}$) can be evaluated from

$$\frac{\partial(R_S + R_D)}{\partial V_{gs}} = \left[\frac{g_{m0}}{g_{d0}} - \frac{g_m}{g_d}\left(1 - \frac{\partial R_D}{\partial V_{ds}}\right)\right.$$
$$\times \left.\vphantom{\frac{g}{g}}\right]\frac{I_d^{-1}}{2 + (g_{m0} + g_{b0}/g_{d0})} \tag{15}$$

The ratio $(g_{m0} + g_{b0})/g_{d0}$ in Eq. (15) can be found by adding the external resistor R_{ext} in series with the source terminal, and then calculating the slope of the reciprocal drain conductance versus R_{ext}. The mathematical expression is given by

$$\frac{g_{m0} + g_{b0}}{g_{d0}} = \frac{\partial g_d^{-1}}{\partial R_{ext}}\left(1 - \frac{\partial R_D}{\partial V_{ds}}\right). \tag{16}$$

The remaining unknown term in Eq. (15), the ratio g_{m0}/g_{d0}, can be obtained at a low drain bias from

$$\frac{g_{d0}}{g_{m0}} = \frac{1 + k}{(g_{m0} + g_{b0})/g_{d0}}, \tag{17}$$

where k is a factor that accounts for the body effect:

$$k = \frac{\partial V_T}{\partial V_{sb}}. \tag{18}$$

Alternatively, the gate-voltage dependence of $(R_D + R_S)$ can be modeled semi-empirically by an expression of the type [28]:

$$(R_S + R_D) = a_0 + \frac{a_1}{a_2 + \left(V_{gs} + V_T\right)}, \tag{19}$$

where the coefficients a_1 and a_2 can be determined by fitting $\partial(R_D + R_S)/\partial V_{gs}$, obtained according to Eq. (15) and plotted as a function of the gate voltage, to the second term on the right-hand side of Eq. (19). The coefficient a_0 represents the total series resistance $(R_D + R_S)$ that is gate-voltage independent. Based on this concept, Guo et al. [18] developed a model for the gate-bias dependent $(R_D + R_S)$:

$$(R_S + R_D) = R_0 + 0.5\left[\alpha\left(V_{gs} - V_T\right)^{-\beta}\right]$$
$$+ 0.5\left[\alpha\left(V_{gs} - V_T - V_{ds}\right)^{-\beta}\right], \tag{20}$$

where α and β are the channel doping concentration dependent parameters, R_0 is a residual resistance at

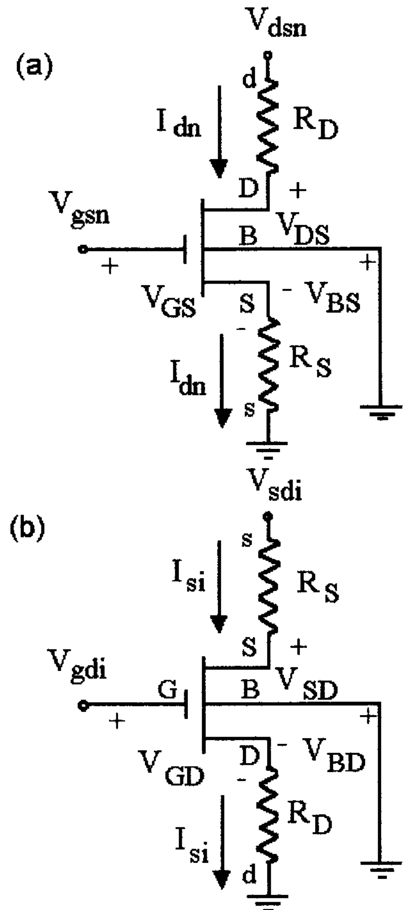

Fig. 7. (a) MOSFET in normal mode of operation with the source and body grounded, and (b) MOSFET in inverse configuration with the drain and body grounded.

very high gate voltages. Note that the second term on the right-hand side of Eq. (20) represents the gate-voltage dependent R_S, and the third term on the right-hand side of Eq. (20) represents the gate- and drain-voltage dependent R_D, which is analogous to the second term when the MOSFET is operating in the linear region (i.e., V_{ds} is small).

3. The difference between the drain and the source series resistances

It is a common practice to assume that the parasitic resistances associated with the drain and source regions of MOSFETs are approximately equal to each other, $R_D \approx R_S$. Therefore, knowing $(R_D + R_S)$, we obtain $R_S \approx R_D \approx (R_S + R_D)/2$. However, this assumption becomes invalid when the drain and source regions of the device are not totally symmetrical. Such an asymmetry results in a difference in the drain and source resistances $(R_D - R_S)$ and can affect considerably the current–voltage characteristics of MOSFETs.

The difference in the drain and source resistances arises mainly from processing, layout, and/or electrical stressing, and it becomes more prominent in the case of deep-submicron devices. This is because the relative importance of the parasitic resistances over the intrinsic components is increased as the geometry of the device shrinks. Previous numerical simulations [13,31] indicate that the drain and source resistance asymmetry is originated mainly from the difference in the drain and source contact resistances, and not from the gate misalignment, nor from the difference in source and drain doping densities.

An approach frequently used for extracting $(R_D - R_S)$ consist on performing measurements of an MOS device, first connected in the 'normal configuration' in which the source and body are grounded, and then measuring it again in the 'inverted configuration' in which the source and drain terminals are interchanged, as shown in Fig. 7(a) and (b), respectively. Two extraction methods, namely the reciprocal transconductance method and gate-voltage shift method, have been developed based on this approach and are presented below.

3.1. Reciprocal transconductance method

The difference between the drain and source resistances, $(R_D - R_S)$, can be extracted from the extrinsic gate transconductance of a single MOSFET measured under saturation operation at the same drain to source voltage but two different configurations. First, the extrinsic gate transconductance g_{mn} for the normal mode of configuration is measured from the I_{dn} versus V_{gsn} characteristics in the saturation region (i.e., the subscript 'n' represents the normal mode of configuration in which the source and body are grounded (Fig. 7(a)). This transconductance is given by

$$g_{mn} = \frac{\partial I_{dn}}{\partial V_{gsn}}. \tag{21}$$

Second, the gate transconductance g_{mi} for the inverse mode of configuration is measured from the I_{si} vs. V_{gdi} characteristics in the saturation region, (i.e., where subscript 'i' represents the inverse mode of configuration in which the source and drain functions are interchanged (Fig. 7(b)). Analogous to Eq. (21), such a transconductance is

$$g_{mi} = \frac{\partial I_{si}}{\partial V_{gdi}}. \tag{22}$$

Applying Eq. (10) to both modes of configuration yields

$$\frac{g_{m0}}{g_{mn}} = 1 + (g_{m0} + g_{b0})R_S + g_{d0}(R_S + R_D) \quad (23)$$

and

$$\frac{g_{m0}}{g_{mi}} = 1 + (g_{m0} + g_{b0})R_D + g_{d0}(R_S + R_D). \quad (24)$$

It should be noted that the intrinsic variables are the same for both modes of configuration, and only R_S and R_D asymmetry is present in the device. Subtracting Eq. (23) from Eq. (24) we obtain:

$$(R_D - R_S) = \frac{(1/g_{mi}) - (1/g_{mn})}{1 + (g_{b0}/g_{m0})}. \quad (25)$$

We stress that the body effect has been included in the denominator of Eq. (25) by retaining the intrinsic body transconductance.

If the body transconductance in Eq. (25) is negligible, that the equation can be approximated by [32]:

$$(R_D - R_S) = \frac{1}{g_{mi}} - \frac{1}{g_{mn}}. \quad (26)$$

However, this expression would only provide a rough estimate of the drain and source resistance asymmetry, since neglecting the intrinsic body transconductance in the saturation region is not generally justifiable and may result in a large error [33,34].

We conclude from Eq. (25) that, in addition to measuring the normal and inverse extrinsic gate transconductances in saturation, it is necessary to know the ratio of the intrinsic body transconductance to the intrinsic gate transconductance (i.e., g_{b0}/g_{m0} term in the denominator of Eq. (25)) before $(R_D - R_S)$ can be determined. Three different procedures to calculate this term have been developed and are presented below.

3.1.1. Variable external resistor procedure

In 1995, Raychaudhuri and co-workers [29,35,36] proposed the following method. A variable external resistor (VER) is connected alternatively in series with the source (denoted by R_{xS}) and with the drain (denoted by R_{xD}) terminals (i.e., $R_{xS} = R_{xD} \equiv R_{xV}$). The gate transconductance of the device, in the normal mode of configuration (source and body grounded), is then measured under these two connections, at the same drain current and several different values of R_{xV}. Using Eq. (10), the reciprocals of the two transconductances $(1/g_{mn})_{R_{xS}}$ and $(1/g_{mn})_{R_{xD}}$ can be expressed by

$$\left(\frac{1}{g_{mn}}\right)_{R_{xS}} = \frac{1}{g_{m0}} + (R_S + R_{xS})\left(1 + \frac{g_{b0}}{g_{m0}}\right) + \frac{g_{d0}}{g_{m0}}(R_D + R_S + R_{xS}), \quad (27)$$

for the connection where the VER is connected to the source, and

$$\left(\frac{1}{g_{mi}}\right)_{R_{xD}} = \frac{1}{g_{m0}} + R_S\left(1 + \frac{g_{b0}}{g_{m0}}\right) + \frac{g_{d0}}{g_{m0}}(R_D + R_{xD} + R_S), \quad (28)$$

for the connection where the VER is connected to the drain.

Whenever g_{m0}, g_{d0} and g_{b0} can be assumed to be roughly constant within the range of the measurement, these two normal-mode gate transconductances would be linear functions of R_{xV}. In that case, when plotted versus R_{xV}, these conductances can be fitted to straight lines. It then follows from Eqs. (27) and (28) that subtracting the slopes of the two resulting straight lines produces the term $(1 + g_{b0}/g_{m0})$ needed in Eq. (26) to calculate the drain and source resistance asymmetry:

$$1 + \frac{g_{b0}}{g_{m0}} = \text{slope of } \left(\frac{1}{g_{mn}}\right)_{R_{xS}} - \text{slope of } \left(\frac{1}{g_{mn}}\right)_{R_{xD}}. \quad (29)$$

3.1.2. Constant external resistor procedure

We propose in this subsection a simpler alternative procedure to obtain the term $(1 + g_{b0}/g_{m0})$ in Eq. (26). This is done by measuring the two extrinsic gate transconductances, as before, but with a single constant external resistor (CER) (i.e., $R_{xS} = R_{xD} \equiv R_{xC}$), instead of a variable one. Taking the difference between the two reciprocal transconductances, given in Eqs. Eqs. (27) and (28), and dividing this difference by the value of the external resistance, we obtain

$$1 + \frac{g_{b0}}{g_{m0}} = \frac{\left(\frac{1}{g_{mn}}\right)_{R_{xS}} - \left(\frac{1}{g_{mn}}\right)_{R_{xD}}}{R_x}. \quad (30)$$

The CER procedure is advantageous in that it only uses a fixed value external resistor, it does not need the straight-line approximation used in the VER procedure and, therefore, it does not require the assumption of constant g_{m0},g_{d0} and g_{b0}.

3.1.3. Extrinsic body transconductance procedure

We also propose in this subsection another alternative method to obtain the term $(1 + g_{b0}/g_{m0})$ in Eq. (26). This term can be also extracted without measurements involving any, variable or fixed, external resistors connected to the source or to the drain terminals. The procedure consists of performing a direct measurement of the extrinsic body transconductance (EBT) g_{bn} in the normal mode configuration, as defined by

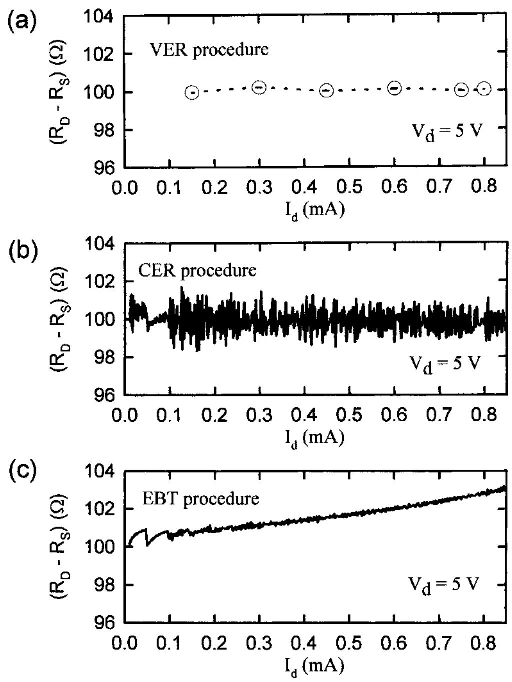

Fig. 8. Extracted difference between the drain and source resistance using the reciprocal transconductance method with three different procedures: (a) VER, (b) CER, and (c) EBT.

$$g_{bn} = \frac{\partial I_{dn}}{\partial V_{bsn}}, \tag{31}$$

or the extrinsic body transconductance in the inverse mode configuration, g_{bi}, as defined by

$$g_{bi} = \frac{\partial I_{si}}{\partial V_{bdi}}. \tag{32}$$

Using Eq. (10) in the normal and inverse mode configurations, the ratio of the intrinsic body transconductance to the intrinsic gate transconductance can be expressed as:

$$\frac{g_{b0}}{g_{m0}} \approx \frac{g_{bn}}{g_{mn}} \approx \frac{g_{bi}}{g_{mi}}. \tag{33}$$

The EBT procedure is simpler to use in the sense that it does not need of any external resistor, nor does it rely on a straight-line fitting scheme. However, as will be shown later, such a procedure is sensitive to the current level and produces the largest error among the three procedures.

3.1.4. Comparison of the three procedures

The VER, CER, and EBT procedures of the reciprocal transconductance method will now be compared to establish the relative merits. Results of $(R_D - R_S)$ for an n-channel MOSFET were extracted using the AIM-SPICE level-10 simulation and the three above-mentioned procedures.

The transistor's parameters used in simulation were: a surface mobility of 331.5 cm^2 V^{-1}s^{-1}, a substrate doping density of 10^{17} cm^{-3}, a metallurgical junction depth of 0.43 μm, an oxide capacitance of 1.38×10^{-7} F cm^{-2}, a threshold voltage of 1 V, a bulk mobility of 331.5 V^{-1} cm^2 s^{-1}, and asymmetrical drain and source resistances of $R_S = 100$ Ω and $R_D = 200$ Ω (i.e., the correct extracted value for $(R_D - R_S)$ should be 100 Ω). The extraction was performed in the saturation region at a drain voltage of 5 V, and different values of drain current up to 1 mA. Fig. 8 shows the calculated R_D and R_S asymmetries obtained by applying the three procedures.

Eight different values of the variable resistor R_{xV} ranging from 5 to 160 Ω were used, for the VER procedure, to calculate the slopes of the straight-line fitted reciprocal transconductance versus R_x. The data points shown in Fig. 8(a) correspond to the resulting $(R_D - R_S)$, extracted in this way at only six representative values (circled in Fig. 8(a)) of drain current because of the lengthy fitting and slope calculations involved. For the CER procedure, a single value of $R_{xC} = 10$ Ω was used. Because no straight-line fitting is necessary, the resistance asymmetry was calculated at every point of the operating drain current, about 500 values in this case, as shown in Fig. 8(b). Similarly, for the EBT procedure, the body transconductance was obtained at every point of operating drain current under the normal configuration, using a body voltage variation of δV_{bsn}, and $(R_D - R_S)$ was calculated and is shown in Fig. 8(c).

The VER procedure produces the smallest maximum extraction error, of around 0.1%, compared against the correct value of $(R_D - R_S) = 100$ Ω, because it includes an averaging step inherent to the straight-line fitting scheme. The results of the CER procedure exhibit a random maximum error of about 2%, which is within a typical range of error for measurements. If a data smoothing step were included in the CER procedure, as that inherented in the VER procedure, the extraction accuracy would be similar to that of the VER procedure. On the other hand, the EBT procedure, which requires measuring the body transconductance directly, presents a progressive error that increases with increasing drain current level, up to around 3% at 1 mA in this case. This can be attributed to the fact that a higher current results in a larger voltage drop in the drain and source resistances, and that the EBT procedure is sensitive to such a voltage drop.

3.2. Gate-voltage shift method

This method is also based on measuring a single transistor when it is connected alternatively in the normal and inverse configurations [37,38]. The difference is that, instead of measuring the difference between normal and inverse reciprocal gate transconductances, it is based on measuring the shift of the gate voltage needed to maintain the same magnitude of drain current when the device is connected in the inverse and normal configurations. Consider a MOSFET in the normal configuration, with the source and body grounded, and also in the inverse configuration, with the drain and source interchanged. The drain current in (I_{dn}), in the normal configuration, can be expressed as a general function of the intrinsic voltages as

$$I_{dn} = f\left[(V_{GS} - V_{Tn}), V_{DS}\right], \tag{34}$$

where f is a function defined by a particular MOSFET model, V_{Tn} is the threshold voltage in the normal configuration, and the body voltage dependence has been implicitly incorporated. The function f does not make any other a priori assumptions as to the model describing the relationship between drain current and applied voltages. The intrinsic gate-to-source and drain-to-source voltages can be expressed, from Eqs. (1) and (2), in terms of their extrinsic counterparts as

$$V_{GS} = V_{gsn} - I_{dn} R_S \tag{35}$$

and

$$V_{DS} = V_{dn} - I_{dn}(R_S + R_D) \tag{36}$$

where V_{gsn} and V_{dsn} represent the extrinsic gate-source and drain-source voltages, respectively, in the normal configuration. In a similar manner, the source current in the inverse configuration is given by

$$I_{si} = f\left[(V_{GD} - V_{Ti}), V_{SD}\right], \tag{37}$$

where V_{Ti} is the threshold voltage in the inverse configuration, and V_{GD} and V_{SD} are the intrinsic gate-drain and source-drain voltages, respectively. These voltages can be related to their extrinsic counterparts by

$$V_{GD} = V_{gdi} - I_{si} R_D \tag{38}$$

and

$$V_{SD} = V_{sdi} - I_{si}(R_S + R_D), \tag{39}$$

where V_{gdi} and V_{sdi} are the extrinsic gate-drain and source-drain voltages, respectively, in the inverse configuration. If the device in both configurations is biased with the same source-drain voltage (i.e., $V_{sdi} = V_{dsn}$) and V_{gdi} is adjusted until the source current in the inverse configuration is equal to that in the normal configuration (i.e., $I_{si} = I_{dn} \equiv I_d$), then the normal and

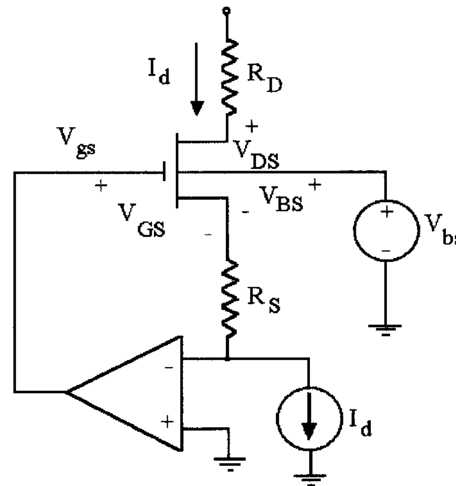

Fig. 9. Circuit for measuring the change of threshold voltage with the body-source voltage at a constant drain current.

inverse intrinsic gate voltage overdrive must be the same:

$$(V_{GS} - V_{Tn}) = (V_{GD} - V_{Ti}). \tag{40}$$

Substituting Eqs. (35) and (38) into Eq. (40) yields

$$I_d(R_D - R_S) = \left(V_{gdi} - V_{gsn}\right) - (V_{Ti} - V_{Tn}). \tag{41}$$

The term $(V_{Ti} - V_{Tn})$ in the above equation is small, when the device is biased in the linear region, because $(V_{DB} - V_{SB})$ is small. Therefore, it can be approximated by the first term of its Taylor series expansion as

$$(V_{Ti} - V_{Tn}) \approx I_d(R_D - R_S)\frac{dV_T}{dV_{SB}}. \tag{42}$$

Combining Eqs. (41) and (42) gives

$$(R_D - R_S) = \frac{\left(V_{gdi} - V_{gsn}\right)/I_d}{1 + (dV_T/dV_{SB})}, \tag{43}$$

where the dependence of the threshold voltage on the source-to-body voltage V_{SB} is accounted for by the term $(1 + dV_T/dV_{SB})$ in Eq. (43). To obtain such a dependence, one can measure the dependence of the gate voltage on V_{SB} instead. This is because the drain current is proportional to V_{gs} and V_T as

$$I_d \propto V_{gs} - I_d R_S - V_T. \tag{44}$$

Thus, at a constant drain current,

$$\frac{dV_T}{dV_{sb}} = \frac{dV_{gsn}}{dV_{sb}}. \tag{45}$$

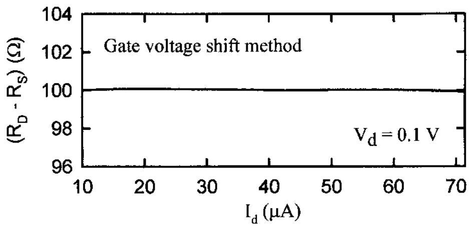

Fig. 10. Extracted difference between the drain and source resistance using the gate-voltage shift method.

Substituting Eq. (45) into (43), we obtain

$$(R_D - R_S) = \frac{\left(V_{gdi} - V_{gsn}\right)/I_d)}{1 + \left(dV_{gsn}/dV_{sb}\right)}. \tag{46}$$

The denominator of Eq. (46) can be obtained by measuring the gate voltage change needed to respond to a small change in the body voltage in order to maintain the same drain current. This term can be easily determined using a circuit involving an operational amplifier shown in Fig. 9.

The calculated difference between the drain and the source resistance, using the gate-voltage shift method, is presented in Fig. 10 using simulated results from AIM-SPICE level-10 model for the same n-channel MOSFET used in Fig. 8. The transistor's parameters are the same as those indicated in Section 3.1.4, including asymmetrical source and drain resistances of $R_S = 100\ \Omega$ and $R_D = 200\ \Omega$. The extraction was performed in the linear region of operation at a drain voltage of 100 mV, and for 360 values of drain current up to 70 μA. Clearly, the method is very accurate, as the simulated $(R_D - R_S)$ is identical to that specified in AIM-SPICE. We have simulated another n-channel MOSFET using AIM-SPICE level-1 and level-10 models in order to illustrate the effects of the term dV_{gsn}/dV_{sb} in Eq. (46) on the accuracy of the gate-voltage shift method. The MOS transistor's parameters used here were the same as before, except that the asymmetrical source and drain resistances in this case are $R_S = 10\ \Omega$ and $R_D = 20\ \Omega$ (i.e., the correct value of $(R_D - R_S)$ is 10 Ω). The threshold voltage dependence on the source-to-body voltage, $dV_{Tn}/dV_{SB} = dV_{gsn}/dV_{sb}$, was first simulated as a function of drain current, from the circuit in Fig. 9, using AIM-SPICE level-1 and level-10 models. A constant value of 0.73 is obtained using the level-1 model, corresponding to the same value that could be calculated using the conventional MOSFET theory: $dV_{Tn}/dV_{SB} = 2 \in qN_A/C_{ox}$ [39]. The more comprehensive level-10 model yields a higher dV_{Tn}/dV_{SB}, rising from 1 to 2.4 as the drain current increases from 0 to 15 μA.

We show in Fig. 11 the values of $(R_D - R_S)$ extracted using AIM-SPICE level-1 and level-10 models and the gate-voltage shift method, with and without including the effects of dV_{Tn}/dV_{SB}. The results indicate that, if the effects of dV_{Tn}/dV_{SB} are not accounted for, the gate-voltage shift method is erroneous and becomes MOSFET model dependent. On the other hand, when the body-voltage dependence is included, the correct result of 10 Ω is obtained, and the extraction method becomes independent of the type of model selected for simulation.

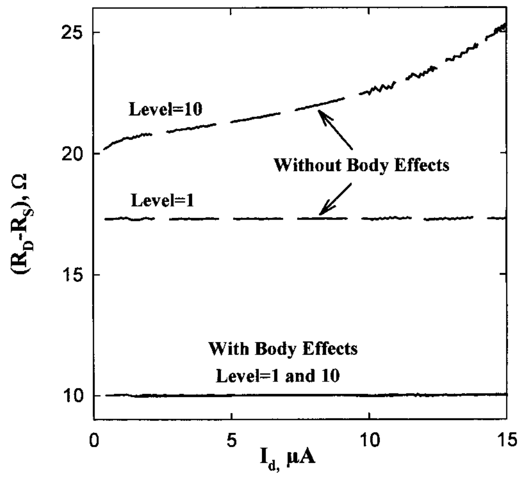

Fig. 11. Extracted difference between the drain and source resistance using the gate-voltage shift method with and without considering the body effect factor. The extraction was carried out in the circuit simulator AIM-SPICE with level-1 and level-10 MOSFET models and $R_S = 10\ \Omega$ and $R_D = 20\ \Omega$.

4. Conclusion

We have reviewed, compared and scrutinized various methods to extract the individual values of the drain and source resistances (R_D and R_S) of MOSFETs. We have stressed the implicit assumptions and limitations of each method and we have proposed variations in order to improve them. These methods have been tested and compared in the environments of a circuit simulator, a device simulation and experimental measurements.

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