



New procedure for the extraction of basic a-Si:H TFT model parameters in the linear and saturation regions

A. Cerdeira^{a,*}, M. Estrada^a, R. García^a, A. Ortiz-Conde^{a,1},
F.J. García Sánchez^b

^a *Departamento de Ingeniería Eléctrica, Sección de Electrónica del Estado Sólido (SEES), CINVESTAV, Av. IPN No. 2508, Apto. Postal 14-740, 07300 DF, Mexico*

^b *Laboratorio de Electrónica del Estado Sólido, Universidad Simón Bolívar, Apartado Postal 89000, Caracas 1080A, Venezuela*

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Abstract

A new procedure is proposed to extract basic parameters for the AIM-Spice amorphous thin film transistor model in the above-threshold region. Our method avoids non-linear optimization, which is mainly the method utilized up to now, when using a program extractor included in AIM-Spice. The present extraction procedure is based on the integration of the experimental data current. The integration method as in known is convenient to decrease the effects of experimental noise. The method is applied to the linear and saturation regions for the above-threshold regime and allows the extraction of all the above-threshold parameters. The accuracy of the simulated curves using the parameters extracted with the new procedure is verified with measured and calculated data using the expressions contained in the model. © 2001 Elsevier Science Ltd. All rights reserved.

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1. Introduction

A universal model for amorphous transistors (a-Si:H TFT) [1–3] has been implemented in AIM-Spice level 15 model [4]. However the number of parameters requested by this model is high. Those related to geometrical and technological factors are not difficult to determine. They are the overlap capacitance (CGSO and CGDO), the oxide thickness (TOX), dielectric constant of the oxide (EPSI) and the substrate layer (EPS) and zero-bias leakage current (IOL). Others parameters related to the trap distribution and intrinsic layer impurity concentration, as the Fermi level position (DEF0), the minimum density of deep states (GMIN) and the characteristic

voltage for deep states (V0), can be estimated from physical ideas and procedures previously reported [1–3]. The other 18 parameters must be also determined, but the way to do it is not straightforward. AIM-Spice provides, as an additional program, a parameter extractor, which tries to optimize several of these parameters at the same time, in order to fit simulated curves to experiment. This is usually troublesome and a satisfactory fit of both simulated $I_{DS}-V_{GS}$ and $I_{DS}-V_{DS}$ curves to experimental curves using this extractor is not always possible to achieve for the same set of model parameters.

Recently, a direct extraction method was proposed in Ref. [5]. However the proposed method has two problems. First, the extraction of the mobility variation parameters is done using the slope of the log–log characteristic. Because the threshold voltage is unknown a high variation of the slope is possible. Second, the extraction of another parameter, m , is made using graphical method, which is neither practical nor precise. The extraction of R is not considered.

*Corresponding author. Tel.: +525-747-3780; fax: +525-747-7114.

E-mail address: cerdeira@mail.cinvestav.mx (A. Cerdeira).

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In this article we present a new method to extract all above-threshold parameters of the a-Si:H TFT AIM-Spice level 15 model. They are determined from the transfer and output characteristics of the transistor without non-linear optimization or graphical data processing. Using the extracted parameters $I_{DS}-V_{GS}$ and $I_{DS}-V_{DS}$ curves were calculated using model expressions and also simulated in AIM-Spice. Both results are compared with the experiment.

2. Basic features of the a-Si:H TFT level 15 model in AIM-Spice

The following expressions for the above-threshold regime in the AIM-Spice level 15 model [4] will be used in the new extraction procedure presented. The drain current in the linear and saturation regions are expressed as:

$$I_{DS} = \frac{K/V_{AA}^\gamma}{1 + R(K/V_{AA}^\gamma)(V_{GS} - V_T)^{1+\gamma}} \times \frac{(V_{GS} - V_T)^{1+\gamma} V_{DS} (1 + \lambda V_{DS})}{\left[1 + \left[\frac{V_{DS}}{V_{DSsat}}\right]^m\right]^{1/m}}, \quad (1)$$

where $K = (W/L)C_i\mu_0$; W , channel width; L , channel length; C_i , gate capacitance; μ_0 , band mobility; V_T , threshold voltage; R , source plus drain resistance; γ and V_{AA} , empirical parameters defining the variation of mobility with V_{GS} ; m , sharpness of the knee region and λ , channel length modulation.

Eq. (1) neglects the leakage current and is the result of considering that the field effect mobility increases with the gate voltage as:

$$\mu_{FET} = \mu_0 \left(\frac{V_{GS} - V_T}{V_{AA}} \right)^\gamma. \quad (2)$$

The intrinsic channel conductance g_{chi} , for the low drain voltage (linear region) is expressed as:

$$g_{chi} = \frac{W}{L} C_i \mu_{FET} (V_{GS} - V_T) = \frac{W}{L} C_i \mu_0 \frac{1}{V_{AA}^\gamma} (V_{GS} - V_T)^{1+\gamma}. \quad (3)$$

The drain current in the linear region (for small drain voltage) from Eq. (1) and for $V_{GS} > V_T$ is written as:

$$I_{DSlin} = \frac{K}{V_{AA}^\gamma} (V_{GS} - V_T)^{1+\gamma} V_{DS}. \quad (4)$$

To take into account the series resistance at drain R_D and source R_S , the effect of the total resistance $R = R_D + R_S$ is introduced in the expression for the channel conductance, obtaining the following expression:

$$g_{chi} = \frac{g_{chi}}{1 + Rg_{chi}}, \quad (5)$$

In a-Si:H TFT transistors the series resistance are high, so the effect introduced by R can be significant even at relatively low currents.

The drain current from Eqs. (3)–(5) is written as:

$$I_{DSlin} = \frac{K/V_{AA}^\gamma}{1 + R(K/V_{AA}^\gamma)(V_{GS} - V_T)^{1+\gamma}} (V_{GS} - V_T)^{1+\gamma} V_{DS}. \quad (6)$$

The saturation voltage is defined through the saturation modulation parameter α_S , which is usually less than 1:

$$V_{DSsat} = \alpha_S (V_{GS} - V_T). \quad (7)$$

The sharpness of the knee region of transition between linear and saturation regions is defined by m .

For $V_{DS} = V_{GS} > V_{DSsat}$, the saturation current from Eq. (1) can be approximated by:

$$I_{DSsat} = \frac{K}{V_{AA}^\gamma} \alpha_S (V_{GS} - V_T)^{2+\gamma}. \quad (8)$$

3. Extraction procedure

The procedure is divided into five steps.

Step no. 1: For a-Si:H TFTs, parameters γ and V_{AA} are extracted from Eq. (4) in the linear region. These parameters may vary from one to another transistor, and are highly dependent on technology. Considering the exponential behavior of Eq. (4), the integral procedure proposed in Ref. [6] is applied, in this case, to the linear region to extract V_T , and γ . The function $H(V_{GS})$ is defined as [6]:

$$H(V_{GS}) = \frac{\int_0^{V_{GS}} I_{DS}(x) dx}{I_{DS}(V_{GS})}. \quad (9)$$

After performing the integration and dividing by I_{DS} the following expression is obtained:

$$H(V_{GS}) = \frac{1}{2 + \gamma} (V_{GS} - V_T). \quad (10)$$

V_T is obtained from the intercept, and γ from the slope of the linear region of Eq. (10) for $V_{GS} > V_T$.

Because this method involves an integral function, it will give better results since it is more immune to problems related with the experimental noise. Another important feature is that it is not necessary to know V_T in order to determine γ .

Step no. 2: Using Eq. (4) the expression $I_{DS}^{1/(1+\gamma)}$ vs. V_{GS} is obtained. After calculating the slope S_1 of the expression $I_{DS}^{1/(1+\gamma)}$ vs. V_{GS} , the value of V_{AA} can be extracted from

$$V_{AA} = \left[\frac{KV_{DS}}{S_1^{1+\gamma}} \right]^{1/\gamma} \quad (11)$$

In this manner the three parameters that determine the effective change of the field effect mobility (Eq. (2)) are extracted with the above-described procedure.

Step no. 3: The drain and source series resistance, R , can be extracted evaluating Eq. (6) at the maximum value of gate voltage. Using this procedure, R is extracted for values of the current in which its effect becomes more important.

Step no. 4: The next step in the extraction procedure uses the saturation current characteristic for $V_{GS} = V_{DS}$. The expression $I_{DS\text{sat}}^{1/(2+\gamma)}$ vs. $(V_{GS} - V_T)$ is obtained from Eq. (8) and its slope S_S is calculated. Parameter α_S is extracted as

$$\alpha_S = \frac{S_S^{2+\gamma} V_{AA}^\gamma}{K} \quad (12)$$

Step no. 5: The values of parameters m and λ can be extracted from the expression for the output current characteristic, Eq. (1). Parameter m is determined at the saturation voltage (Eq. (7)) and its value is obtained from

$$m = \log 2 / \log \left[\frac{K}{V_{AA}^\gamma} \frac{\alpha_S (V_{GS} - V_T)^{2+\gamma}}{I_{DS\text{sat}} (V_{DS\text{sat}})} \right] \quad (13)$$

Finally, the channel length modulation parameter λ is extracted evaluating Eq. (1) at the maximum values of V_{DS} and V_{GS} voltages to fit the slope of the experimental data.

With this five steps procedure, all parameters included in the above-threshold model, V_T , γ , V_{AA} , R , α_S , m and λ are extracted. The default values are assigned for the rest of the model parameters.

Some authors [7] use the concept of field effect mobility μ_{FET0} as the value of the mobility extracted from the approximated saturation current formula:

$$I_{DS\text{sat}} = \frac{W}{L} C_i \frac{\mu_{FET0}}{2} (V_{GS} - V_T)^2 \quad (14)$$

This value is normally used to evaluate the fabrication process. Comparing Eq. (8) with Eq. (14), a value for μ_{FET0} can be obtained in function of the extracted parameters as shown in the following expression:

$$\mu_{FET0} \approx \mu_0 \frac{\alpha_S^2}{V_{AA}^\gamma} \quad (15)$$

4. Extraction example

An a-Si:H TFT with stacked structure and Cr gate, drain and source contacts, fabricated in our laboratory,

was used to demonstrate the extraction procedure. The technological data is: SiO₂ gate thickness = 300 nm; intrinsic layer thickness = 300 nm; channel width = 600 μm and channel length = 40 μm. A typical transistor was used. The band mobility parameter μ_0 was taken equal to its default value, 10 cm²/Vs.

The experimental data corresponding to the transfer characteristic in the linear region at $V_{DS} = 0.1$, was mathematically processed following step no. 1. The following parameters were extracted: $V_T = 5.6$ V; $\gamma = 0.324$. Following step no. 2, the value of $V_{AA} = 35240$ V was obtained, and following step no. 3 the value of $R = 1700$ Ω was obtained.

The linear characteristic calculated using Eq. (4) is compared with the experimental data in Fig. 1.

The extracted parameters V_T , γ and V_{AA} were used, following step no. 4 in conjunction with the experimental data from the current in the saturation region (Eq. (8)) in order to extract the value of $\alpha_S = 0.47$ (Eq. (11)).

The experimental data of the output characteristic was processed according to step no. 5 to obtain $m = 2.2$ at $V_{GS} = 30$ V using Eq. (13). Finally the value of $\lambda = 1.76 \times 10^{-3}$ 1/V was calculated.

In Fig. 2 the experimental data is compared with the output characteristic calculated using Eq. (1) and with the simulated using AIM-Spice. Both calculated and simulated are practically the same and fit well the experimental data, validating the proposed new extraction method.

As already mentioned, the procedure also allows the calculation of the value of mobility μ_{FET0} substituting the extracted parameters in Eq. (15). A value of $\mu_{FET0} = 0.32$ cm²/Vs was obtained. Fig. 3 shows the mobility variation according to Eq. (2), where the value corresponding to μ_{FET0} is indicated.

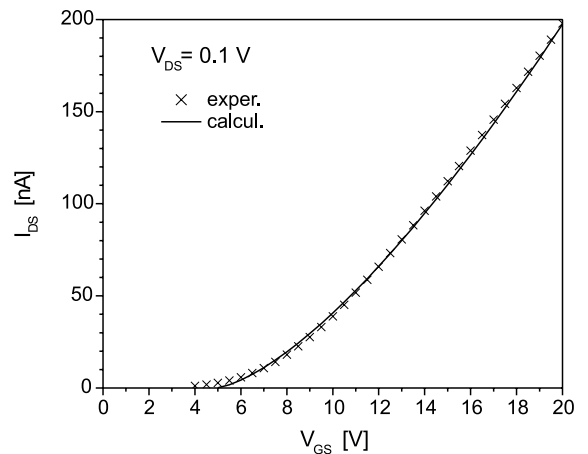


Fig. 1. Experimental and calculated I_{DS} - V_{GS} characteristic for $V_{DS} = 0.1$ V.

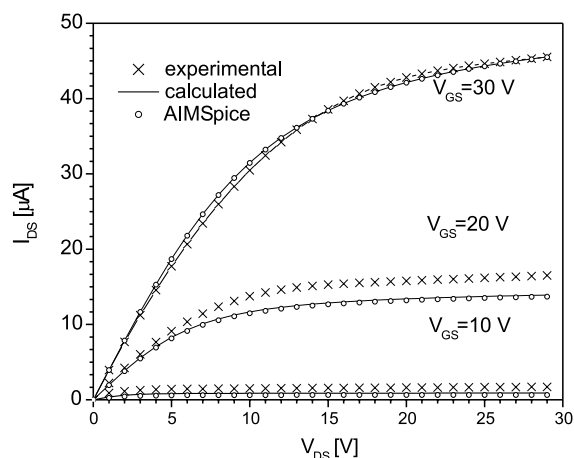


Fig. 2. Experimental, calculated and simulated with AIM-Spice I_{DS} – V_{DS} characteristics for $V_{GS} = 10, 20$ and 30 V.

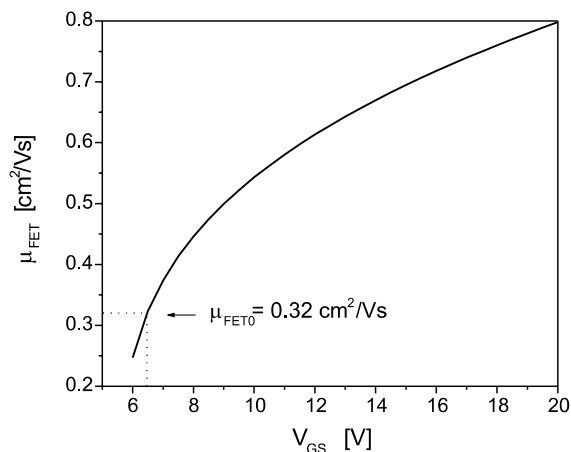


Fig. 3. Dependence of the field effect mobility on gate voltage. The value of μ_{FET0} calculated with the extracted parameters is also indicated.

5. Conclusions

The new proposed procedure permits to extract all above-threshold parameters of the level 15 model implemented in AIM-Spice, without non-linear optimization or graphical methods. The values of V_T and the exponent γ can be extracted independently one from the other using one single mathematical processing involving an integral method that additionally reduces experimental noise. No graphical methods or non-linear optimization are needed to calculate any of the parameters. The extraction of the total source-and-drain series resistance is included.

Comparison of experimental I_{DS} – V_{GS} and I_{DS} – V_{DS} with calculated transfer and output curves using model expressions (Eqs. (1), (4) and (8)), to the simulated curves in AIM-Spice using the extracted parameters shows good match, thus, validating the proposed procedure.

References

- [1] Lee K, Shur M, Fjeldly T, Ytterdal T. Semiconductor Device Modeling for VLSI. New Jersey: Prentice Hall; 1993.
- [2] Shur M, Slade H, Jacunski M, Owusu A, Ytterdal T. SPICE models for amorphous and polysilicon thin film transistors. J Electrochem Soc 1997;144(8):2833–9.
- [3] Fjeldly T, Ytterdal T, Shur M. Introduction to device modeling and circuit simulation. New York: Wiley; 1998.
- [4] AIM-Spice, Circuit simulation program by AIM-Software. www.aimspice.com.
- [5] Slade H. Device and material characterization and analytic modeling of amorphous silicon thin film transistors. PhD thesis, University of Virginia, 1997.
- [6] Ortiz-Conde A, Cerdeira A, Estrada M, García Sánchez FJ, Quintero R. A simple procedure to extract the threshold voltage of amorphous thin film transistors in the saturation region, Solid-State Electron, submitted for publication.
- [7] Cheon B, Jin Y, Hyun J, Jang J. Hydrogenated amorphous silicon thin film transistor fabricated on plasma treated silicon nitride. IEEE Trans Electr Dev 2000;ED-47(2):367–71.