



A simple procedure to extract the threshold voltage of amorphous thin film MOSFETs in the saturation region

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Abstract

A technique is presented to extract the threshold voltage of amorphous thin film MOSFETs in the saturation region. The technique is proposed because threshold voltage extraction in amorphous TFTs is different, and in general more complex, than in conventional crystalline bulk devices, since these TFTs exhibit several notable dissimilarities inherent to their characteristics. The saturation drain current follows an m power-law type dependence on gate bias, with an m different from the conventional value of 2. Additionally, a plot of the saturation current as a function of gate bias does not reveal the existence of an inflexion point. The method presented, which extracts the value of the power-law parameter m as well, is based on the use of an auxiliary operator that involves the integration of the drain current as a function of gate voltage. The technique was tested and its accuracy verified using the measured characteristics of an experimental n-channel a-Si:H thin film MOSFET. © 2001 Published by Elsevier Science Ltd.

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1. Introduction

Many methods have been reported [1–13] to extract the threshold voltage, V_T , of a MOSFET. Recently two books [1,2] and three articles [3–5] have reviewed and scrutinized the different methods available. Additionally, five more methods [9–13] have been proposed during the past three years. Almost all of these methods extract V_T from the measured drain current, I_D , versus the gate bias, V_G , in the linear region of operation. To the best of our knowledge, only one method [1] is available to extract V_T in the saturation region, based on linearly extrapolating the $I_D^{1/2}$ versus V_G plot at the inflexion point to the gate bias axis.

Some available methods [6,10,11] entail using the derivative of the drain current with respect to the gate bias. The main disadvantage of using such methods is that the effect of experimental errors is magnified by the computation of the derivative. Two other methods [9,13] have been published which are based, instead, on the integration of the drain current with respect to the gate bias. Using such an integration procedure offers the inherent advantage of reducing the effects of experimental errors.

The extraction of V_T in amorphous MOSFETs is more conveniently performed from the drain current in saturation, considering that these devices present much smaller currents than conventional devices. Amorphous TFTs introduce the following additional difficulties for V_T extraction: First, the saturation drain current in strong inversion is usually modeled by an equation of the form [14]

$$I_{D\text{sat}} = K(V_G - V_T)^m, \quad (1)$$

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where K is a conductance parameter with units of $A V^{-m}$ and m an empirical parameter which can be different from 2, the value used in conventional MOSFET models. Second, the value of parameter m cannot be easily extracted from a simple plot of $\log(I_{D\text{sat}})$ versus $\log(V_G)$ because practical operation values of V_G are usually not large enough to validate the approximation: $(V_G - V_T) \approx V_G$. Third, it is not clear at what point the $I_{D\text{sat}}$ versus V_G plot could be linearly extrapolated, since the curve does not present an inflexion point because the mobility of these devices raises as V_G is increased. Parameter extraction through direct optimization is not a good alternative either, because of the difficulties that arise due to the m power-law type dependence on gate bias.

To circumvent some of these difficulties, we will next present the new method to extract the threshold voltage of amorphous thin film MOSFETs, based on the integration of the saturation current with respect to the gate bias.

2. Parameter extraction method

Lets define the following function which can be numerically computed from the measured $I_{D\text{sat}}(V_G)$ characteristics:

$$H(V_G) = \frac{\int_0^{V_G} I_{D\text{sat}}(V_G) dV_G}{I_{D\text{sat}}}, \quad (2)$$

where the upper limit of integration is any value greater than the threshold voltage.

We now wish to obtain an analytical approximation for $H(V_G)$. We first break up the integral in Eq. (2) into two distinct parts

$$H(V_G) = \frac{\int_0^{V_T} I_{D\text{sat}}(V_G) dV_G + \int_{V_T}^{V_G} I_{D\text{sat}}(V_G) dV_G}{I_{D\text{sat}}}. \quad (3)$$

If we select values of V_G such that the device is operating in the strong inversion region, the contribution of the first integral in Eq. (3) is negligible and, thus, $H(V_G)$ may be approximated by the second part,

$$H(V_G) \approx \frac{\int_{V_T}^{V_G} I_{D\text{sat}}(V_G) dV_G}{I_{D\text{sat}}}. \quad (4)$$

After substitution of Eq. (1) into Eq. (4), and assuming that the variation of K with respect to V_G is insignificant, we obtain:

$$H(V_G) = \frac{(V_G - V_T)}{m + 1}, \quad (5)$$

which means that $H(V_G)$ is linear in the strong inversion region. Therefore, a plot of function $H(V_G)$ has a slope

that defines the value of m and a V_G axis intercept which gives the sought after value of V_T .

The complete extraction procedure basically consists of three steps: (a) numerically evaluate $H(V_G)$, as defined by Eq. (2), using the measured $I_{D\text{sat}}(V_G)$ characteristics; (b) do a straight-line fit of the $H(V_G)$ plot in the strong inversion region and extract the values of m and V_T from its slope and V_G axis intercept, respectively, according to Eq. (5); and (c) after having found m and V_T , the remaining parameter in Eq. (1), K , may be easily evaluated from:

$$K = \frac{I_{D\text{sat}}}{(V_G - V_T)^m}. \quad (6)$$

3. Experimental validation and discussion

The new extraction procedure was applied to an experimental n-channel a-Si:H thin film MOSFET with a structure as illustrated in Fig. 1. The relevant fabrication parameters are: a gate oxide thickness of 0.3 μm ; an intrinsic a-Si:H layer thickness of 0.3 μm ; 0.1 μm thick n^+ drain and source regions with impurity concentrations of 10^{18} cm^{-3} ; channel width of 600 μm and length of 40 μm . The measured I_D versus V_{DS} characteristics for several values of V_G are presented in Fig. 2. Examination of this figure allows us to deduce that the threshold voltage must be smaller than 10 V, since the characteristics show that already at $V_G = 10$ V there is a reasonable current flowing.

Fig. 3 presents the measured $I_{D\text{sat}}$ and calculated $g_{m\text{sat}} = dI_{D\text{sat}}/dV_G$ versus V_G using linear and logarithmic scales for the vertical axis. The current was mea-

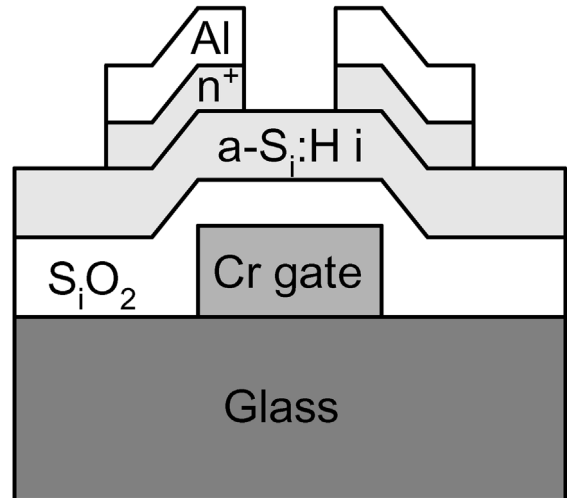


Fig. 1. Schematic device structure of the experimental amorphous TFT.

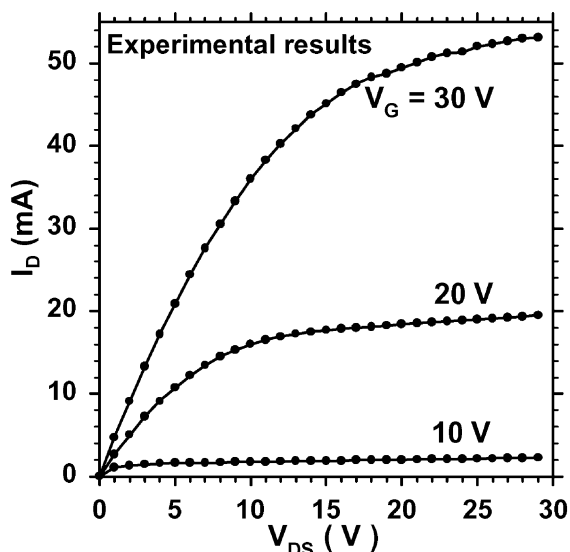


Fig. 2. Measured I_D – V_{DS} characteristics at three values of gate bias for the experimental n-channel amorphous TFT.

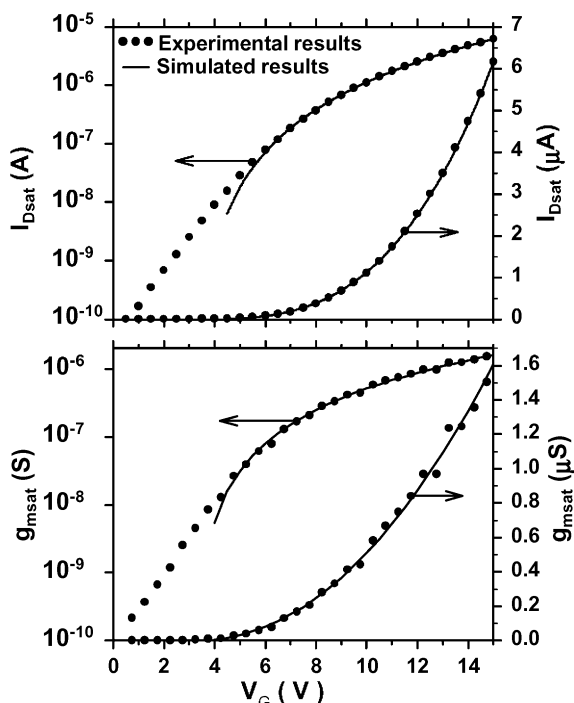


Fig. 3. Measured I_{Dsat} and the resulting $g_{m,sat} = dI_{Dsat}/dV_G$ (●) versus gate bias for the experimental n-channel amorphous TFT. A 0.5 V gate-to-source voltage step was used with the drain connected to the gate. Also shown (—) are the simulated results using the extracted set of parameter values: $m = 3.07$, $V_T = 3.25$ V and $K = 3.2$ nA V $^{-m}$.

sured using 0.5 V gate-to-source voltage steps, with the drain connected to the gate. Fig. 3 also presents the results of the simulation using Eq. (1) with the values of parameters that will be extracted in this section. It is clear from this figure that the plot of I_{Dsat} does not show evidence of any inflexion point and, thus, the plot of $g_{m,sat} = dI_{Dsat}/dV_G$ is seen to always rise as V_G is increased. If we were to apply the commonly used so-called “constant current definition” for threshold voltage as being the gate bias corresponding to an arbitrary value of drain current, for instance 0.1 μ A, we would obtain $V_T = 6$ V, a value which is far from being correct, as we shall see. Likewise, using the plot of $\log(I_{Dsat})$ versus V_G would give the false impression that the transition from weak to strong inversion occurs at about 8 V, a value that is an even worse estimation of the threshold voltage.

Fig. 4 illustrates the importance of the power-law empirical exponent, m , by presenting the saturation current normalized with the respect to its maximum value raised to the power of $1/m$, for several values of m . This plot should be a straight line with a V_G axis intercept equal to V_T when the correct value of m is used. We may conclude from the various curves that it is unclear what the correct value of m is. The same can be said of the extracted value of V_T , since it is evident that it is strongly dependant on the selected value of m .

Fig. 5 presents a plot of the numerical calculation of $H(V_G)$ using Eq. (2). For strong inversion the curve is seen to behave approximately as a straight line with a slope of 0.246 and a V_G axis intercept (threshold voltage) of 3.25 V. Furthermore, according to Eq. (5), this slope implies a power-law empirical exponent $m = 3.07$. It is worth noting here that an alternate but laborious way to extract m for the strong inversion region would be to find, through trial and error, the value of m which

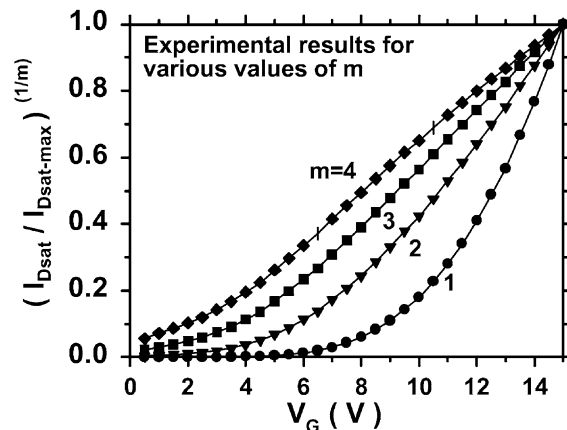


Fig. 4. Experimental saturation current normalized with respect to its maximum value raised to the $1/m$ power versus gate bias for various values of m .

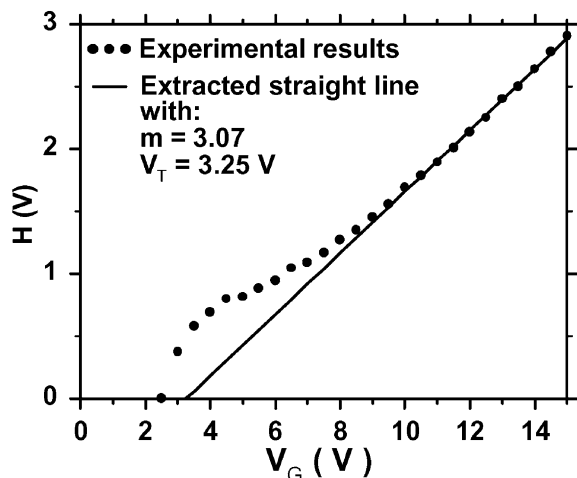


Fig. 5. Function $H(V_G)$ calculated for the I_D - V_G characteristics of the device of Fig. 2. The slope of the straight line for strong inversion is 0.246, which according to Eq. (5) implies $m = 3.07$. The intercept of the straight line to the gate bias axis is 3.25 V, which implies $V_T = 3.25$ V.

produces the maximum linearity of $I_{Dsat}^{1/m}$, evaluated through a linear regression coefficient. Such procedure was applied and it yields $m = 3.06$, with a linear regression coefficient of 0.999797, which matches very well the value previously extracted through the present procedure and thus confirms its accuracy.

Finally, Fig. 6 shows the plot of K extracted by using Eq. (6) for the strong inversion region. From this figure we find that $K = 3.2 \text{ nA V}^{-m}$, within a relative experimental variation of less than 2%.

In order to validate the extraction procedure, synthetic I_{Dsat} and dI_{Dsat}/dV_G versus V_G curves were simulated using Eq. (1) with the set of extracted parameter

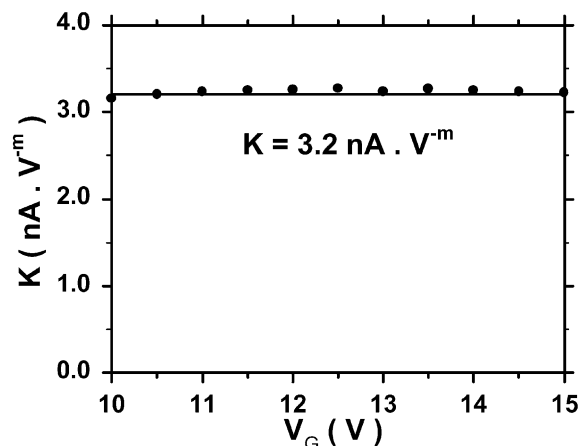


Fig. 6. Extracted value of $K = 3.2 \text{ nA V}^{-m}$ using Eq. (6) for the strong inversion region. The relative experimental variation of this extracted value is less than 2%.

values: $m = 3.07$, $V_T = 3.25$ V and $K = 3.2 \text{ nA V}^{-m}$. Both curves are presented in Fig. 3 together with their corresponding experimental data. The figure clearly shows that the simulations using the extracted parameters approximate very well the measured data for strong inversion.

4. Conclusions

We have presented a new simple method to extract the threshold voltage of amorphous thin film transistors in the saturation region, a task that is more complicated in this type of devices than in conventional MOSFETs. The method proposed is based on the integration of the current with respect to the gate bias in strong inversion. In addition to the threshold voltage, the new method is capable of extracting the empirical constant m . The procedure was tested by using it to extract the parameters of an experimental n-channel a-Si:H thin film MOSFET. The excellent fit obtained between the resulting characteristics, simulated using the extracted parameters, and the experimental data validate the procedure. Because of the low-pass filter nature of integration, this method offers the additional advantage of inherently reducing the effects of experimental errors.

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References

- [1] Schroeder DK. Semiconductor material and device characterization, 2nd ed. New York: Wiley; 1998.
- [2] Liou JJ, Ortiz-Conde A, García Sánchez FJ. Analysis and design of MOSFETs: modeling, simulation and parameter extraction. New York (USA): Kluwer Academic Publishers; 1998.
- [3] Liou JJ, Ortiz-Conde A, García Sánchez FJ. Extraction of the threshold voltage of MOSFETs: an overview (invited). Proc IEEE HKEDM, Hong Kong, June 1997. p. 31–8.
- [4] Terada K, Nishiyama K, Hatanaka KI. Comparison of MOSFET threshold voltage extraction methods. Solid-State Electron 2001;45:35–40.
- [5] Ortiz-Conde A, García Sánchez FJ, Liou JJ. An overview on parameter extraction in field effect transistors. Acta Científica Venezolana 2000;51:176–87.
- [6] Wong HS, White MH, Krutsick TJ, Booth RV. Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFET's. Solid State Electron 1987;30:953.

- [7] Jain S. Measurement of threshold voltage and channel length of submicron MOSFETs. *IEE Proc Circ Dev Syst* 1988;135:162.
- [8] Yan ZX, Deen MJ. Physically-based method for measuring the threshold voltage of MOSFETs. *IEE Proc Circ Dev Syst* 1991;138:351.
- [9] Ortiz-Conde A, Gouveia E, Liou JJ, Hassan MR, García Sánchez FJ, De Mercato G, Wang W. A new approach to extract the threshold voltage of MOSFETs. *IEEE Trans Electron Dev* 1997;ED-44:1523–8.
- [10] Tsuno M, Suga M, Tanaka M, Shibahara K, Miura-Mattausch M, Hirose M. Reliable threshold voltage determination for sub-0.1 μm gate length MOSFETs. *Proc Asia South Pacific Conf* 1998. p. 111–6.
- [11] Dobrescu L, Petrov M, Dobrescu D, Ravariu C. Threshold voltage extraction methods for MOS transistors. *Proc Int Sem Conf* 2000. p. 371–4.
- [12] Tan C, Xu M, Wang Z. Proportional difference operator method and its application in studying subthreshold behavior of MOSFETs. *Solid-State Electron* 2000;44:1059–67.
- [13] García Sánchez FJ, Ortiz-Conde A, Mercato GD, Salcedo JA, Liou JJ, Yue Y. New simple procedure to determine the threshold voltage of MOSFETs. *Solid-State Electron* 2000;44:673–5.
- [14] Merckel G, Rolland A. A compact CAD model for amorphous silicon thin film transistors simulation-I. D.c. analysis. *Solid-State Electron* 1996;39:1231–9.