

# A Minimal Integral Nonlinearity Criterion to Optimize the Design of a New tanh/sinh-Type Bipolar Transconductor

Francisco J. García Sánchez, *Senior Member, IEEE*, Adelmo Ortiz-Conde, *Senior Member, IEEE*, Jesús L. Finol, *Member, IEEE*, Ramón B. Salazar, and Javier A. Salcedo, *Member, IEEE*

**Abstract**—We report on the use of a simple design optimization criterion for obtaining maximum static transfer function linearity. It is based on an analytic function that corresponds to the integral nonlinearity of the circuit. The criterion may be useful, either as an analytic tool to gain insight into the circuit's behavior, or as an efficient computational alternative to calculating total harmonic distortion (THD). It is utilized here to optimize the design parameters of a recently proposed bipolar transconductor capable of high linearity, which is composed of two parallel-connected nonlinear blocks: a *hyperbolic tangent-type* transconductor and *hyperbolic sine-type* transconductor. Examination of this tanh/sinh-type transconductor concept, using the analytic version of the present criterion, indicates that this new circuit configuration is theoretically capable of achieving values of THD lower than possible with conventional bipolar *hyperbolic tangent-type* transconductors. A particular design example is presented to demonstrate, through simulations, the performance of the new transconductor, and in order to ascertain the ability of the proposed design optimization criterion for obtaining maximum static transfer function linearity. In this particular example, THD values of less than 0.3% are obtained with a 100- $\mu$ S transconductance up to a maximum input voltage swing of 50-mV peak.

**Index Terms**—Design optimization, integral nonlinearity, tanh/sinh-type bipolar transconductor, total harmonic distortion.

## I. INTRODUCTION

TRANSCONDUCTOR circuits are the basic components of operational transconductance amplifiers (OTA) and are also commonly used in active filter design [1], [2]. The use of bipolar-type transconductor circuits [3] allows a wide tunability range because of the exponential dependence of the current on the base-emitter voltage of bipolar junction transistors (BJTs). However, one of the major limitations of the conventional bipolar “*hyperbolic tangent-type*” transconductor is that in order to maintain linearity the maximum differential input voltage swing that is allowed is very small, of the order of the thermal voltage. Basically, two ideas have been traditionally used to circumvent this limitation: The first and most common is the multi-tanh [4] configuration, where two or more *hyperbolic*

*tangent-type* conventional differential amplifiers, each with a certain base offset voltage, are simply connected in parallel. The second is the “externally linear internally nonlinear” concept (ELIN) [5], [6], based on some sort of configuration consisting of nonlinear networks internally connected to produce an externally linear result. Following the general motivation of this second concept, Finol and Lovelace recently proposed [7] to use a circuit composed of the parallel combination of a “*hyperbolic sine-type* differential amplifier” [5], [8], [9] and a conventional *hyperbolic tangent-type* differential amplifier [10]. The rationale is that, since the second derivatives of the sinh and tanh functions present opposite signs (sinh and tanh have expansive and compressive behaviors, respectively), a circuit based on the addition of these two functions could conceivably be designed to be linear for a larger input voltage swing than either one of the tanh-type or sinh-type differential amplifiers.

In what follows, we describe a procedure to be used for designing the circuit that implements this new bipolar tanh/sinh-type transconductor concept. The goal of the design criterion is to obtain a tanh/sinh-type transconductor which exhibits the maximum static transfer function linearity possible, for given maximum input voltage swing and desired transconductance. Therefore, the essence of the optimization criterion must be to minimize the amount of static nonlinearity introduced by the circuit. To this end, instead of relying on the cumbersome conventional “brute-force” calculation of the circuit's total harmonic distortion (THD) by iteratively sweeping the relevant design parameters and performing a fast Fourier transformation for each step in order to determine the parameter values which minimize it, we propose to use an alternative new simple optimization approach that can be applied either in one analytical step, or numerically by iteration. The new approach is based on the use of the “difference integral function”  $D$  [11], [12] which has already been successfully used for other types of applications, such as procedures to suppress linear parasitic terms in device parameter extraction [13],[14]. Function  $D$  defines the area between the circuit's actual static transfer function and an ideal straight line drawn through its end points. As such, it represents a measure of the circuit's static integral nonlinearity (INL) [15] and it is, therefore, directly related to distortion. Recently, [16] this concept was successfully used to quickly measure the harmonic distortion in SOI MOSFET devices and differential pairs. In order to corroborate the validity of the proposed criterion for design optimization purposes, the new tanh/sinh-type transconductor is optimized

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F. J. García Sánchez, A. Ortiz-Conde, R. B. Salazar, and J. A. Salcedo are with Laboratorio de Electrónica del Estado Sólido, Universidad Simón Bolívar, Caracas 1080A, Venezuela (e-mail: fgarcia@ieee.org).

J. L. Finol is with the Semiconductor Products Sector, Motorola, Phoenix, AZ 85018 USA (e-mail: jlfinol@ieee.org).

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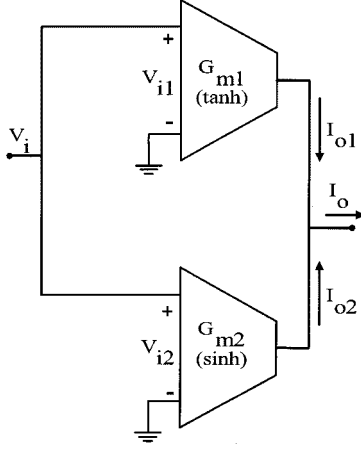


Fig. 1. Proposed tanh/sinh-type transconductor's block diagram showing the parallel combination of a tanh-type transconductor and a sinh-type transconductor.

using this procedure and its results compared to conventional direct numerical optimization methods based on minimizing THD. The industry standard statistical language S-plus [17] is used for this purpose.

## II. ANALYTICAL CRITERION IN THE IDEAL CASE

Fig. 1 presents the proposed transconductor's block diagram, which shows the parallel combination of a tanh-type transconductor block (represented by  $G_{m1}$ ) and a sinh-type transconductor block (represented by  $G_{m2}$ ). The combined total output current of the new bipolar tanh/sinh-type transconductor is ideally given by

$$I_O = I_{O1} + I_{O2} = I_n \left[ a \tanh\left(b \frac{V_i}{2V_{th}}\right) + c \sinh\left(d \frac{V_i}{2V_{th}}\right) \right] \quad (1)$$

where  $V_i$  is the input voltage,  $V_{th}$  is the thermal voltage, parameters  $a$  and  $c$  are arbitrary positive real numbers that scale  $I_n$ , which is a normalized common bias current, and parameters  $b$  and  $d$  are input voltage attenuation coefficients, that could be implemented by a variety of passive or active networks.

The task at hand is to find, for a given maximum voltage swing and desired transconductance, the values of the four parameters ( $a$ ,  $b$ ,  $c$ , and  $d$ ) in the previous equation, such that the resulting static transfer characteristics will exhibit maximum linearity. As stated above, the condition for maximum linearity may be found using the conventional approach of repeatedly performing fast Fourier transformations to determine the parameter values which minimize THD. Simple observation, backed by numerical optimization results using S-plus programming, indicate that the lowest THD values are obtained in the present circuit configuration when the smallest practical values of  $b$  and  $d$  are used to attenuate the input signal. This logical result is independent of the values of  $a$  and  $c$  and can be easily understood by realizing that decreasing  $b$  and  $d$  implies reducing the arguments of both hyperbolic functions in (1). However, practical considerations, fabrication and otherwise, usually impose that neither one of the attenuation coefficients  $b$  and  $d$  may be

smaller than a certain practical limiting value, say  $1/F$ , dictated mainly by fabrication technology and area limitation considerations. Accordingly, we shall use values of  $b$  and  $d$  equal to whatever minimum is allowed by practical limitations, that is,

$$b = d = \frac{1}{F}. \quad (2)$$

We need now to determine the optimum values of parameters  $a$  and  $c$ . Let us denote by  $V_m$  the maximum input voltage swing to be expected according to the specifications, and let's design for a certain average transconductance,  $G$ , desired within this given maximum input voltage range  $-V_m < V_i < V_m$ . Taking the derivative of  $I_o$  with respect to  $V_i$ , the average transconductance can be expressed as

$$G \equiv \frac{1}{V_m} \int_0^{V_m} \frac{dI_O}{dV_i} dV_i = \frac{1}{V_m} [I_O(V_i = V_m) - I_O(V_i = 0)]. \quad (3)$$

Then, substituting (1) and (2) into (3) we get

$$G = \frac{I_n}{V_m} [a \tanh(v_{nm}) + c \sinh(v_{nm})] \quad (4)$$

where

$$v_{nm} \equiv \frac{V_m}{F2V_{th}} \quad (5)$$

is defined for convenience as the normalized maximum input voltage swing. Solving (4) for  $(cI_n)/G$  as a function of  $(aI_n)/G$ , we get an expression that defines the relationship that must exist between  $a$  and  $c$  to obtain the average transconductance  $G$ , for a given maximum input voltage swing,  $V_m$ , using the maximum input attenuation,  $F$ , allowed by practical fabrication considerations

$$\frac{cI_n}{G} = \frac{V_m - \frac{aI_n}{G} \tanh(v_{nm})}{\sinh(v_{nm})}. \quad (6)$$

We now need to find a second relationship between  $a$  and  $c$ . To do that, we must apply a maximum linearity design criterion, but instead of trying to minimize the THD through numerical optimization of  $a$  and  $c$ , we will seek, as proposed in the introduction, an analytical solution by evaluating the circuit's static transfer function integral nonlinearity using function  $D$  [11], [12] which for this purpose is defined as

$$D \equiv \int_0^{I_O} V_i dI_O - \int_0^{V_i} I_O dV_i = V_i I_O - 2 \int_0^{V_i} I_O dV_i. \quad (7)$$

Because the operator  $D$ , as defined above, has the property of canceling any linear terms present in the function on which it operates,  $D$  is ideally suited to measure integral nonlinearity which is directly related to THD. For example, if  $I_O$  were a perfectly linear function of  $V_i$ ,  $D$ , and similarly THD, would be exactly equal to zero. Therefore, in order to maximize the static linearity of the present circuit, the function  $D$  of its static transfer characteristics should be as close to zero as possible. Proceeding to

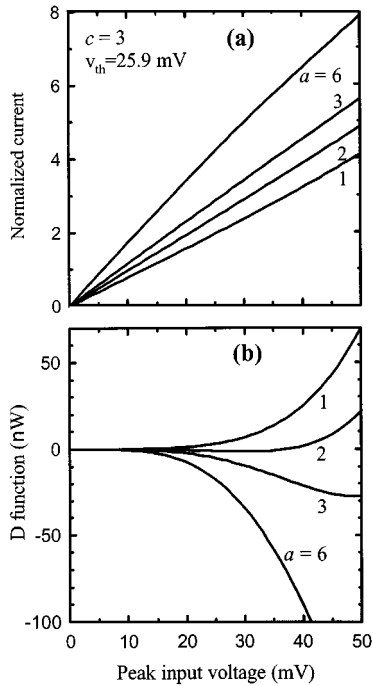


Fig. 2. (a) Normalized current ( $I/I_n$ ), calculated from (1) f. (b) Function  $D$ , evaluated with (8), versus peak input voltage  $V_i$ ; for a fixed value of  $c = 3$  and four possible values of  $a$ .

that end, substituting (1) and performing the integration in the last term of (7) yields the expression of  $D$  for this ideal circuit

$$D = I_n V_i \left[ a \tanh \left( \frac{V_i}{F2V_{th}} \right) + c \sinh \left( \frac{V_i}{F2V_{th}} \right) \right] - 2FI_n 2V_{th} \left\{ a \ln \left[ \cosh \left( \frac{V_i}{F2V_{th}} \right) \right] + c \left[ \cosh \left( \frac{V_i}{F2V_{th}} \right) - 1 \right] \right\}. \quad (8)$$

To visualize the effect on the static transfer characteristics of this tanh/sinh-type transconductor of changing its design parameters, Fig. 2 presents plots of normalized current  $I/I_n$ , calculated from (1), and the resulting  $D$ , calculated using (8), versus peak input voltage  $V_i$  up to 50 mV, for a hypothetical case of a maximum attenuation factor  $F = 1$  (i.e.:  $b = d = 1$ ), a fixed arbitrary value of  $c = 3$  and four possible values of  $a = 1, 2, 3$ , and 6. We notice that, although the output currents appear approximately linear for the four cases, as expected  $D$  is initially very close to zero near  $V_i = 0$ , later increasing to finally end up rising exponentially for large values of  $V_i$ . In two of the cases ( $a = 3$  and 6), which correspond to compressive behavior of the output current, the exponential rise (not visible in the figure) occurs after having  $D$  become negative and gone through a maximum negative value. On the contrary, for the two other cases ( $a = 1$  and 2), which correspond to expansive behavior of the output current,  $D$  remains always positive. The evolution of  $D$  with varying  $a$ , as revealed by the changing shape of the plots in Fig. 2(b), suggests possible design criteria for choosing the parameters' values that would produce maximum linearity. The strict and universally applicable criterion would be to minimize the cumulative absolute value of  $D$  within the

whole input voltage range. This criterion will be applied numerically in the last Section of this paper for comparison purposes. However, its use for deducing analytic expressions of the optimum parameter values would entail unnecessary complexity. Instead, we will use an alternative criterion consisting of making  $D$  become zero at the maximum specified input voltage swing  $V_i = V_m$ . Applying such a condition is almost identical, for the application at hand, to minimizing the cumulative absolute value of  $D$  within the whole input voltage range, as can be inferred by simple inspection of Fig. 2(b), and will be later confirmed by rigorous simulations. For this particular example of the tanh/sinh transconductor, it is easy to conclude that either criterion would produce an optimum value of  $i$  somewhat higher than two.

The fact that the two above-mentioned criteria yield optimum values of  $a$  which are insignificantly different from each other, allows us to use here the second criterion and require that  $D$  should become zero at the maximum specified input voltage swing. Thus, equating (8) to zero at  $V_i = V_m$  and substituting equation (4) into it yields

$$0 = V_m \left( \frac{GV_m}{I_n} \right) - 2F2V_{th} \cdot \{ a \ln[\cosh(v_{nm})] + c[\cosh(v_{nm}) - 1] \}. \quad (9)$$

This equation is the second relationship between  $a$  and  $c$  that we were looking for. We now solve (9) together with the previously found relationship between  $a$  and  $c$ , equation (6), to get the following solutions for the required values of parameters  $a$  and  $c$ :

$$a = \frac{GV_m}{I_n} \frac{\coth(v_{nm}) - \operatorname{csch}(v_{nm}) - \frac{v_{nm}}{2}}{1 - \operatorname{sech}(v_{nm}) - \ln[\cosh(v_{nm})]} \quad (10)$$

and

$$c = \frac{GV_m}{I_n \sinh(v_{nm})} \cdot \left\{ 1 - \frac{\coth(v_{nm}) - \operatorname{csch}(v_{nm}) - \frac{v_{nm}}{2}}{1 - \operatorname{sech}(v_{nm}) - \ln[\cosh(v_{nm})]} \tanh(v_{nm}) \right\}. \quad (11)$$

The above two equations represent the analytic criteria to exactly determine the required coefficients  $a$  and  $c$  that would ideally produce maximum linearity at given specified requirements of: 1) desired average transconductance  $G$ ; 2) maximum expected input voltage range  $V_m$ ; and 3) maximum input attenuation factor  $F$  allowed by practical considerations. It is useful to point out that, although the optimum values of  $a$  and  $c$  do depend on the average transconductance  $G$  desired in each particular design, the ratio  $c/a$  is independent of it. In fact, as evidenced by dividing (10) by (11)

$$\frac{c}{a} = \frac{1 - \operatorname{sech}(v_{nm}) - \ln[\cosh(v_{nm})]}{\sinh(v_{nm})[\coth(v_{nm}) - \operatorname{csch}(v_{nm}) - \frac{v_{nm}}{2}]} - \cosh(v_{nm}) \quad (12)$$

the ratio  $c/a$  results to be only a function of the normalized maximum input  $v_{nm}$ , which, according to (5), includes the thermal voltage, the maximum input voltage range  $V_m$ , and the maximum input attenuation factor  $F$  allowed.

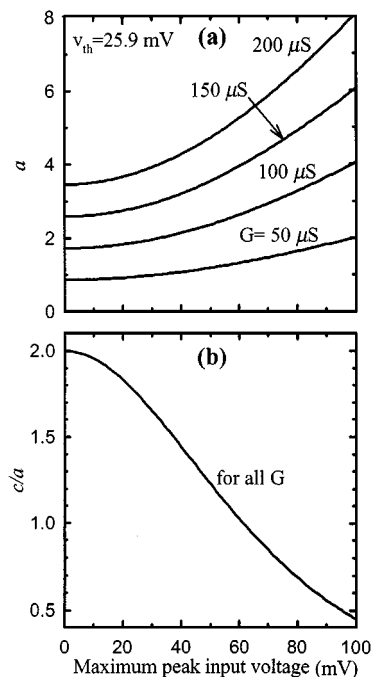


Fig. 3. (a) Optimum values of parameter  $a$  as functions of specified maximum input voltage swing ( $V_m$ ), calculated from (10) and (12), respectively, for four possible values of average transconductance. (b) Corresponding  $c/a$  ratio.

Fig. 3 presents plots of the optimum values of parameter  $a$  and the corresponding ratio  $c/a$ , that would ideally produce maximum linearity, as functions of specified maximum input voltage swing  $V_m$ . They were calculated using (10) and (12), respectively, for a hypothetical attenuation factor of  $F = 1$  and four possible desired values of  $G$ . Fig. 3(a) shows that at each given  $G$  the optimum values of  $a$  increase with increasing  $V_m$ . Fig. 3(b) indicates that the ratio  $c/a$  decreases as  $V_m$  increases, but, as expected from (12), it does so independently of  $G$ . Both trends may be explained by noting that, as the specified  $V_m$  increases, the expansive effect of the *hyperbolic sine* (represented by parameter  $c$ ) becomes more dominant than the compressive effect of the *hyperbolic tangent* (represented by parameter  $a$ ). Therefore, in order to maintain the maximum linearity of the combination, the ratio  $c/a$  must decrease.

### III. APPLYING THE IDEALIZED ANALYTICAL APPROACH

The above procedure will be illustrated by an example of a possible design. Let us assume, for simplicity, an input voltage attenuation factor of  $F = 1$  (i.e.,  $b = d = 1$ ), an expected maximum input voltage swing of  $V_m = 50$  mV, and a target average transconductance of  $G = 100 \mu\text{S}$ . It should be noted that the value of  $F$  does not affect the optimization procedure, since input attenuation is external to the  $\tanh/\sinh$ -type transconductor and therefore the optimum values of  $a$  and  $c$  do not depend on the choice of  $F$ . Then, using (10) and (11), we get:  $a = 2.35$  and  $c = 2.89$  ( $c/a = 1.23$ ), in agreement with (12). Fig. 4(a) presents the resulting normalized total output current ( $I_O/I_n$ ), and its two components, as functions of the peak input voltage  $V_i$ , from zero, going through the value of the designed-for maximum voltage swing  $V_m = 50$  mV, all the way

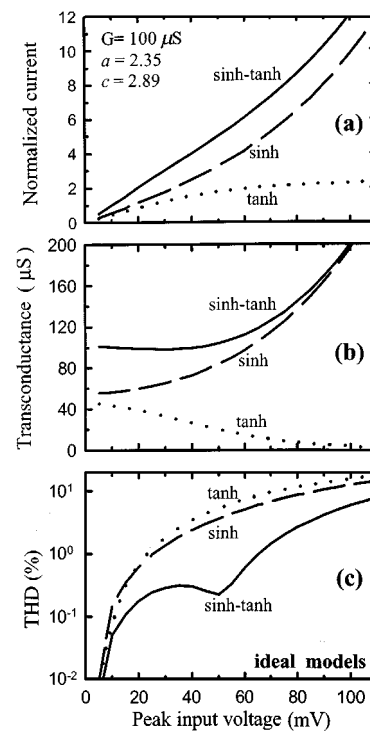


Fig. 4. (a) Total normalized output current ( $I_O/I_n$ ) and of its two components, calculated as functions of the peak input voltage  $V_i$  using ideal device models and the parameters optimized for  $V_m = 50$  mV. (b) The corresponding transconductance of the total circuit and those of its two components. (c) The corresponding THD of the total circuit and of its two component blocks acting separately.

up to  $V_i = 100$  mV. The three plots illustrate how the nonlinearities of the two components compensate each other to produce a normalized output current which is highly linear, as expected, up to the designed-for maximum voltage swing  $V_m$ . The plot of the transconductance,  $d(I_O/I_n)/dV_i$ , shown in Fig. 4(b) confirms that, within the desired input voltage range  $0 < V_i < 50$  mV, the resulting transconductance is indeed in agreement with our design target of an average  $G = 100 \mu\text{S}$ . Fig. 4(c) presents the THD resulting from the total current, and from its two components if they were independently considered. We notice first that the THD corresponding to the new  $\tanh/\sinh$ -type transconductor increases until it reaches a local maximum of about 0.3%, later decreasing slightly to a minimum value of about 0.2% which occurs, as expected, at the designed-for maximum input voltage swing of 50 mV. In contrast to this behavior, we observe that the corresponding THDs of the independent components both increase steadily, reaching values of 6.3% and 3.7% at the specified maximum input voltage swing of 50 mV. This comparison demonstrates the mutual compensation of the expansive and compressive nonlinearities of the  $\sinh$  and  $\tanh$  component blocks, giving rise to a significant reduction of the new  $\tanh/\sinh$ -type transconductor's THD, with respect to what would be achievable by either of the two component blocks operating alone. In the case of this particular example the THD reduction is of at least one order of magnitude.

A question may arise at this point as to whether, instead of the here proposed optimization method, it might not be simpler to use another approach to static linearity optimization such as conventional minimization of the squares of the terms above

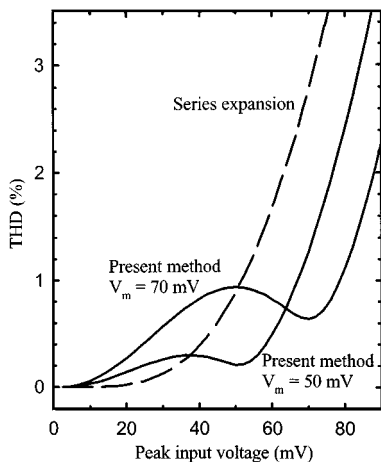


Fig. 5. THD as a function of peak input voltage produced by the circuit designed using the  $c/a$  ratios resulting from conventional series expansion optimization and from the present minimal integral nonlinearity optimization method. Two designs are shown for the present method corresponding to optimizations for two values of maximum peak input voltage  $V_m$ .

the first order of a power series expansion of the static transfer characteristics. To answer this question we will comparatively discuss both approaches. The use of a Taylor series expansion about the origin entails calculating increasing order derivatives rather than just the one integration required by the method proposed here. This is the first comparative strength of the new method. Integration is always preferable to differentiation in any practical situation since it inherently reduces the effect of measurement error and noise, whereas differentiation unavoidably increases this effect. A second and crucial difference between using conventional series expansion optimization and the present procedure is that series expansion necessarily implies that the design is being optimized at just one point of the transfer characteristics, the point about which it is being expanded, which for the case at hand would correspond to zero input voltage. On the contrary, the proposed integral nonlinearity minimization criterion is an overall process in that it optimizes the design globally over the whole operating range, from zero up to the maximum expected input voltage. Minimization of the squared terms of the Mac Laurin series expansion of the  $\tanh/\sinh$ -type transconductor's static transfer characteristics produces an optimum  $c/a$  ratio value equal to that which would be obtained when optimizing with the proposed minimal nonlinearity method for a maximum peak input voltage  $V_m = 0$ .

To clearly visualize the differences between both procedures, we have applied conventional series expansion optimization to the example presented above. Fig. 5 shows the THD as a function of peak input voltage produced by the circuit designed using the  $c/a = 2$  ratio that results from series expansion optimization. We have included in the figure for comparison of the THDs obtained when using two minimal integral nonlinearity optimized designs corresponding to two values of maximum peak input voltage  $V_m$  of 50 mV ( $c/a = 1.23$ ) and 70 mV ( $c/a = 0.84$ ). We observe that, as should be expected, series expansion optimization produces lower THD only close to the series expansion point, that is, at input voltages values close to zero. But as the input voltage increases toward the maximum designed-for value, the present method produces significantly smaller THD.

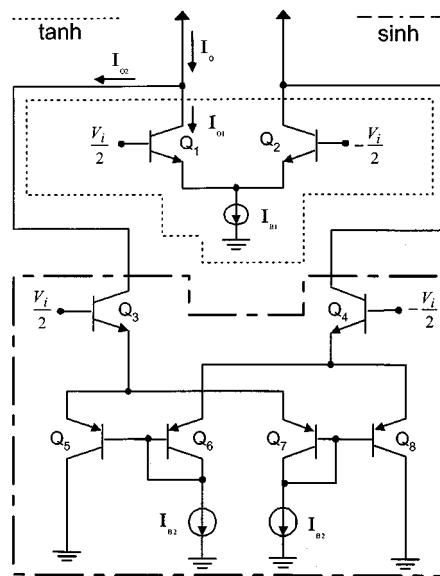


Fig. 6. Circuit architecture of the new  $\tanh/\sinh$ -type transconductor with its two parallel connected constituents enclosed in broken lines: the  $\tanh$ -type transconductor block in the upper part, and the  $\sinh$ -type transconductor block in the lower part.

We might add that the overall THD is also smaller with the present method, as can be verified by calculating the average THD from zero input voltage to  $V_m$ .

It should be emphasized that the difference between the two procedures becomes progressively irrelevant as the maximum input voltage requirement of the particular design tends to zero. This is to be expected since, as already mentioned, minimal integral nonlinearity optimization for values of  $V_m$  close to zero is equivalent to minimizing the squared terms above the first order of a power series expansion about zero. This can be further corroborated by noting that the  $c/a$  ratio value shown in Fig. 3(b) for  $V_m = 0$  in fact corresponds to the value that would be obtained by power series optimization. More importantly however, Fig. 5 indicates that for designs requiring large values of maximum input voltage, the difference between the present procedure and conventional series expansion optimization becomes even greater. Suppose, for instance, that we wish to design a  $\tanh/\sinh$ -type transconductor with average  $G = 100 \mu\text{S}$ , maximum input amplitude up to 70 mV, maintaining the output THD below 1%. Fig. 5 clearly reveals that conventional optimization using series expansion would not fulfill the given requirements, because it would result in THD of up to 2.83%. On the contrary, if the present optimization method were used, THD would be kept below 0.64% at any input amplitude up to the required 70 mV. The decision about what maximum peak input voltage to use for optimizing a particular design obviously depends on the application for which it is intended.

#### IV. CIRCUIT SIMULATIONS

We shall use now the optimum parameter values obtained from the above design criteria, based on the idealized analytical equations of the two transconductor blocks, to perform actual circuit simulations using more realistic and rigorous device

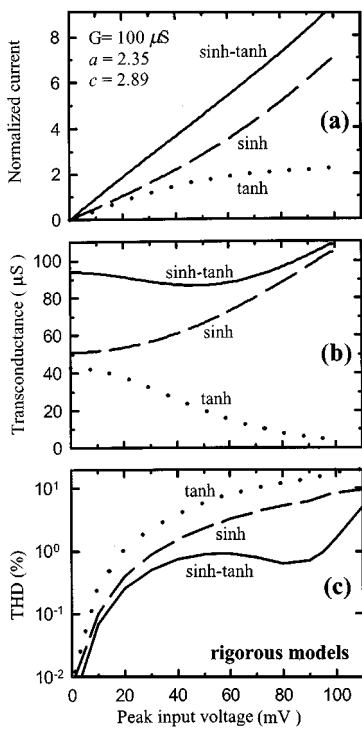


Fig. 7. (a) Total normalized output current ( $I_O/I_n$ ) and of its two components, simulated as functions of the peak input voltage  $V_i$  using rigorous device models and the parameters analytically optimized for  $V_m = 50$  mV. (b) The corresponding transconductance of the total circuit and those of its two components. (c) The corresponding THD of the total circuit and of its two component blocks acting separately.

models. To this end we will consider the basic circuit architecture shown in Fig. 6, which contains a tanh-type transconductor, in its upper part, connected in parallel to a sinh-type transconductor, in its lower part. Notice that we have omitted in the schematic circuit diagram the input attenuation network ( $b = d = 1$ ) and have shown the differential input voltage as  $\pm V_i/2$ . The bias currents shown in the diagram are  $I_{B1} = aI_n$ , and  $I_{B2} = cI_n/2$  when expressed in terms of the normalized current  $I_n$ .

To explore the effect on optimization of using realistic models for the devices, the tanh/sinh-type transconductor circuit was simulated using a new analytic “finite  $\beta$  model” of the sinh-type transconductor, whose description is presented in the Appendix, and also using AIM-SPICE [18] assigning rigorous Gummel–Poon models to all the devices. Typical values used were for the npn transistors:  $I_S = 10^{-18}$  A,  $\beta_F = 100$ ,  $\beta_R = 10$ ,  $V_{AF} = 50$  V, and  $V_{AR} = 2$  V; and for the pnp transistors:  $I_S = 3 \times 10^{-17}$  A,  $\beta_F = 70$ ,  $\beta_R = 10$ ,  $V_{AF} = 100$  V, and  $V_{AR} = 2$  V. The values of parameters  $a$  and  $c$  used in the simulations are those obtained from the idealized analytical optimization results ( $a = 2.35$ ,  $c = 2.89$ , with  $b = d = 1$ ) for the same design target of  $G = 100 \mu\text{S}$  with  $V_m = 50$  mV.

When the transconductor circuit, designed with the values of  $a$  and  $c$  obtained from the idealized analytical optimization criteria, is simulated using either finite  $\beta$  models for the sinh-type transconductor block or rigorous Gummel–Poon models, higher than expected THD’s are obtained. Fig. 7 presents the normalized total current with its two components, and the corresponding transconductances and THD, as functions of the

input voltage  $V_i$ , resulting from rigorous model simulation. These results should be compared to those presented in Fig. 4. Notice that in addition to exhibiting higher overall THD, its minimum has shifted to an input voltage value higher than expected. We may also observe, by comparing Figs. 4(a) and 7(a), that the sinh block part of the total transconductor current has become noticeably straighter than would be expected from a purely sinh behavior. This particular effect can be understood considering the behavior of the sinh-type transconductor block’s finite  $\beta$  model presented in the Appendix. Notice also in Fig. 7(b) that the resulting average transconductance has failed to completely achieve the design target of  $100 \mu\text{S}$ .

## V. ANALYSIS AND DISCUSSION

In order to further investigate the effect of the models used, we performed extensive direct numeric calculations, using the S-plus environment, to the three types of models already mentioned. Simple Ebers–Moll device models, which do not include the effects of Early voltage, were used to produce both the “ideal models” (very large  $\beta$ ) and the “finite  $\beta$  models.” The “rigorous model” was Gummel–Poon’s with the values indicated previously. We applied three optimization procedures based on three types of criteria for quantifying the resulting nonlinearity. All three procedures include simulating the tanh/sinh-type transconductor with varying values of the parameters, using each of the three types of device model already discussed. In the first procedure the THD is calculated and used as the criterion for quantifying and minimizing the resulting nonlinearity. Since this procedure is usually considered conventional, it will be used as reference.

The other two procedures, are proposed as alternative criteria for quantifying the circuit’s nonlinearity, and are both based on the analytic definition of function  $D$ , as given by (7). One is simply a normalized version of  $D$  defined as

$$D_N = \left| 1 - \frac{2 \int_0^{V_m} I_O dV_i}{V_m I_m} \right| \quad (13)$$

where  $I_m = I_O(V_i = V_m)$ . When using this criterion to achieve minimum integral nonlinearity the optimum is said to be reached when  $D_N = 0$ . The absolute value bars in (13) are not really necessary and they are included here only for illustrative consistency. Without them  $D_N$  would just cross from positive to negative values at the minimum nonlinearity condition [recall Fig. 2(b)]. The last is the rigorous and universally applicable criterion that evaluates the cumulative absolute value of  $D$  within the interval of interest, in this case from  $V_i = 0$  up to  $V_m$ . It is defined as

$$D_T = \int_0^{V_m} |D(V_i)| dV_i \quad (14)$$

and the optimum (minimum integral nonlinearity) is achieved when  $D_T$  reaches its minimum value.

The calculation simplicity relative advantage of the proposed alternative  $D$ -based criteria, over the more conventional THD minimization, is specially valuable and attractive when nonlinearity optimization is to be included together with circuit simu-

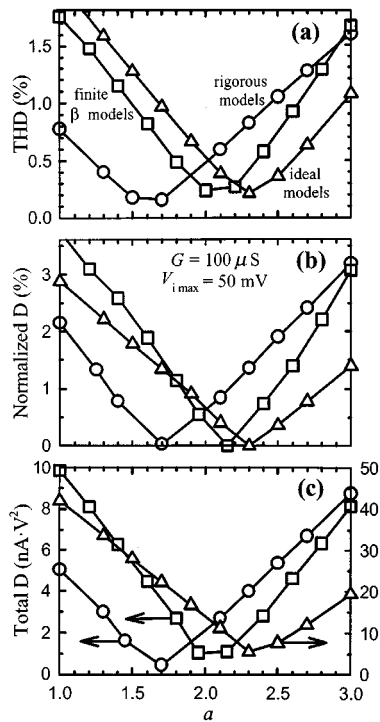


Fig. 8. (a) THD. (b) Normalized  $D$ . (c) Total  $D$  as functions of parameter  $a$ ; calculated from simulations using the same design specifications and three types of device models.

lation within an iterative loop to produce the optimum values of the parameters.

Fig. 8 shows the results of calculating the three versions of the criteria from simulations of the present design, using the same design specifications as already indicated, and three types of device models. Although the optimum value of  $a$ , corresponding to the minima shown, is calculated by numerical optimization, the THD, normalized  $D$ , and total  $D$  resulting from simulations are presented as functions of parameter  $a$  to illustrate their sensitivity to this parameter. The figure clearly confirms that, regardless of the criteria used to describe nonlinearity, numerical optimization using ideal device models, does indeed produce the optimum value of parameter  $a = 2.35$  which was previously predicted by the proposed single-step idealized analytical design criteria, represented by (10) and (11). Additionally, Fig. 8 indicates that either of the three criteria used to describe nonlinearity produce the same optimum value of parameter  $a$ , which turns out to be smaller than the value predicted by the idealized analytical approach when more real device models are used. This offers further evidence that minimizing  $D$ , either normalized or total, is equivalent to minimizing THD.

Finally, it is interesting to note in Fig. 8 that when the value for parameter  $a = 1.7$ , obtained by numerical optimization with rigorous device models, is used this circuit configuration is capable of realistically producing, under the previously stated de-

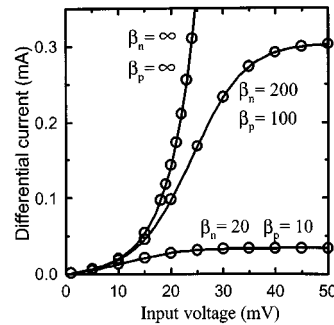


Fig. 9. Output current of the sinh-type transconductor block, calculated from (A1) (continuous lines) and obtained from SPICE simulations (circles), for three combinations of  $\beta_n$  and  $\beta_p$ .

sign specifications, a THD below 0.1% for input voltage swings of up to at least 50-mV peak. Notice that this THD value is only slightly smaller than what was predicted by the analytical design criteria based on ideal device models, which was around 0.2% at the designed-for maximum peak input voltage of  $V_m = 50$  mV and average transconductance of  $100 \mu\text{S}$ . Apparently, the main reason for the improved linearity observed stems from the fact that the sinh-type transconductor block is in reality “more linear” than expected from its ideal behavior, as explained in the Appendix.

## VI. CONCLUSIONS

We have presented a design optimization criterion for obtaining maximum static transfer function linearity, based on an analytic function that corresponds to the integral nonlinearity of the circuit. Because of its relative computational simplicity we have proposed to use it for quantifying nonlinearity, as an alternative to the conventional and more complex calculation of THD. We have applied this criterion, both analytically and numerically, to optimize the design parameters of a new bipolar tanh/sinh-type transconductor. Circuit simulation results, using rigorous device models, demonstrate that actual implementation of the new transconductor can achieve the theoretical expectations, and even surpass them by proper choice of the  $\beta$ s of the devices that make up the sinh-type part of the transconductor.

## APPENDIX

Analysis of extensive simulations of the circuit architecture shown in Fig. 6 indicates that when nonidealized device models are used, the sinh-type transconductor part, and not the conventional tanh-type transconductor part, is chiefly responsible for the linearity behavior of the new tanh/sinh-type transconductor. To try to understand the origin of the observed linearity behavior we have developed a less idealized analytic model for the sinh-type transconductor. Using a device model that includes the effect of finite  $\beta$ , the resulting differential output cur-

$$I_{O2} = \frac{(1 + \beta_p) \{ [\exp(V_i/2v_{th})]^2 - 1 \} (\beta_p + 2) I_{B2} \beta_n}{[1 + \exp(V_i/2V_{th}) + \beta_p \exp(V_i/2V_{th})][1 + \beta_p + \exp(V_i/2V_{th})](1 + \beta_n)} \quad (\text{A1})$$

rent of the sinh-type transconductor, can be expressed as shown in (A1) at the bottom of the previous page, where  $\beta_n$  and  $\beta_p$  correspond to the NPN and PNP devices, respectively. This expression reduces to a pure hyperbolic sine function by letting the  $\beta$ s tend to infinity.

Fig. 9 presents the sinh-type transconductor output current as calculated with (A1) (continuous lines) and as obtained from SPICE simulations (circles), for three combinations of  $\beta_n$  and  $\beta_p$ , including the idealized case when they are assumed to be infinite. We observe in Fig. 9 that as  $\beta$  decreases, the transfer function starts to depart from its ideal sinh-type behavior ( $\beta_n = \beta_p = \infty$ ), in effect becoming “straighter,” until at low values of  $\beta_n$  and  $\beta_p$  it becomes essentially compressive. This new model produces results that match those obtained from simulations and explains the observed nonideal behavior of the sinh-type transconductor circuit.

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**Francisco J. García Sánchez** (M’74–SM’97) was born in Madrid, Spain, on January 20, 1947. He received the B.E.E., M.E.E., and Ph.D. degrees in electrical engineering from the Catholic University of America, Washington, DC, in 1970, 1972, and 1976, respectively.

Since 1977, he has been a Faculty Member of the Electronics Department at Universidad Simón Bolívar (USB), Caracas, Venezuela, where he is presently a Full Professor. In 1987, he created the Solid-State Electronics Laboratory, Caracas, Venezuela, which he has been directing ever since. He has held several academic positions at USB, which include Coordinator of Research and Development for Engineering and Applied Sciences, Coordinator of Undergraduate and Graduate Studies in Electronics Engineering, and Member of the University’s Academic and Superior Councils. He has also held several research and development planning and management positions including Coordinator for the Area of Electronics in Venezuela’s New Technologies National Plan, President of the Engineering and Applied Sciences Commission of the National System for the Promotion of Research and a Member of its Directorate, Member of the External Evaluation Commission of Mexico’s National Institute of Astrophysics, Optics and Electronics (INAOE), Project Evaluator for Venezuela’s CONICIT and Mexico’s CONACYT. He has authored numerous contributed and invited publications and presentations in national and international technical journals and conferences, has been the editor of collective works, and was the coauthor of a recent book on MOSFET modeling. He serves as reviewer for national and international journals and conferences and has been Associate Editor of the journal *Acta Científica Venezolana*. His current research interests are mainly in the area of electrical characterization and modeling of materials and semiconductor devices.

Prof. García Sánchez has been a member of the Steering Committee of the IEEE International Caracas Conference on Devices, Circuits and Systems (IC-CDSC) since 1995, where he has performed duties as its General, Technical Program, Organization, and Local Arrangements Chairperson. He chairs IEEE’s CAS/ED/PE Venezuelan Chapter and is presently the Vice-Chair of the Electron Devices Society Subcommittee for Regions & Chapters for Latin America (SRC-LA). He is a member of the Venezuelan Association for the Advancement of Science, and a Founding Member and Past Vice-President of the Galilean Society. He has been the recipient of several recognition awards for excellence in research.



**Adelmo Ortiz-Conde** (S’82–M’85–SM’97) was born in Caracas, Venezuela, on November 28, 1956. He received the B.S. degree in electronics from the Universidad Simón Bolívar (USB), Caracas, Venezuela, in 1979, and the M.E. and Ph.D. degrees from the University of Florida, Gainesville, in 1982 and 1985, respectively.

From 1979 to 1980, he served as an Instructor in the Department of Electronics at the USB. In 1985, he joined the technical Staff of Bell Laboratories, Reading, PA, where he was engaged in the development of high-voltage integrated circuits. Since 1987, he has been with the Department of Electronics at the USB and was promoted to Full Professor in 1995. He was on sabbatical leave at the Florida International University, Miami, from September to December 1993, and at the University of Central Florida (UCF), Orlando, from January to August 1994, and again from July to December 1998, and at CINVESTAV, Mexico City, Mexico, from October 2000 to February 2001. His doctoral research was in the area of semiconductor device modeling under the guidance of Prof. J. G. Fossum.

He has authored one textbook, *Analysis and Design of MOSFETs: Modeling, Simulation and Parameter Extraction* (Boston, MA: Kluwer, 1998), 52 refereed journal articles (including two invited review articles) and 42 papers (including three invited papers) in international conference proceedings. His present research interest includes the modeling and parameter extraction of semiconductor devices.

Dr. Ortiz-Conde is Member of Eta Kappa Nu, Tau Beta Pi, Phi Kappa Phi and the Galilean Society. He is the Editor of the IEEE EDS NEWSLETTER (REGION 9) and the Vice-Chair of IEEE’s CAS/ED/PE Venezuelan Chapter. He is a Member of the Editorial Advisory Board of Microelectronic and Reliability, and of the Engineering and Applied Sciences Commission of the National System for the Promotion of Research. He has served as Reviewer for national and international journals and conferences. He was the General Chairperson of the first IEEE International Caracas Conference on Devices, Circuits, and Systems in 1995, the Technical Chairperson of the second edition of this conference in 1998, and the Chairperson of the Steering Committee in 2000, and the chairperson of the Technical Committee of the fourth edition of this conference held in Oranjestad, Aruba, in April 2002.



**Jesús L. Finol** (S'76–M'82) received the undergraduate degree in electronics engineering communications, (with honors), from the Federal University of Rio de Janeiro, Rio de Janeiro, Brazil, in 1972, and the Master of Science and Doctor of Philosophy degrees in electrical engineering, from the Georgia Institute of Technology, Atlanta, in 1975, and 1982, respectively.

He was a Professor and Researcher at the Simon Bolívar University (SBU), Caracas, Venezuela from 1972 to 1982, and taught graduate and undergraduate classes and performed research in semiconductor physics, electromagnetic theory, and integrated circuit design. In 1983, he joined Harris Corporation as a Principal Engineer in the Semiconductor Division, and was in charge of R&D of Data Acquisition Architectures, delivering five major designs to production. He was a Visiting Scholar at the University of California at Berkeley in 1985–1986, on leave from Harris Semiconductors, where he performed R&D on special data acquisition architectures, and guided and advised Ph.D. students in the same area. Dr. Finol also worked as a Principal Design Engineer at Intel Corporation, Portland, OR, a Senior Expert at the International Telecommunications Union, Geneva, Switzerland, assigned at the Centre of Research and Development of the Brazilian Telecommunication Company in Campinas, Brazil. He also served as a mentor in IC design for telecommunication systems and established a local IC design capability while in Brazil. Since 1991, he has been a Senior Technical Staff Member with Motorola, Incorporated, Phoenix, AZ, previously as a Design Leader of strategic programs for the Corporation in wireless IC design for cellular telephony, paging systems and two-way radios, and currently as a Chief Scientist and Director of Technology for the Latin America and Caribbean Region of the Semiconductor Products Sector. In his current role, he leads all Regional Technical Activities and Academic Programs. He has been actively involved in R&D and conference activities with Universities throughout the Latin America and Caribbean Region. He has over 20 published papers in national and international conferences and has been awarded nine U.S. patents in integrated circuit design, with three more pending.



**Ramón B. Salazar** was born in Caracas, Venezuela, in 1977. He received the electronics engineering degree from the Simón Bolívar University (SBU), Caracas, Venezuela, in 2001.

He has been a Research Assistant in the field of IC low-noise transconductors for gm-C filter applications at SBU's Solid-State Electronics Laboratory (LEES). He is currently a GSM Systems Development Engineer at Digital Corporation, a cellular telephone services company in Caracas, Venezuela. His main interests are low-noise amplifiers, RF circuits, and IC design for wireless communications systems.

Mr. Salazar's undergraduate senior project "Development of improved analytic models and optimization of transconductors" received the "Mention of Honor" and two subsequent awards from the Venezuelan Society for the Advancement of Science (AsoVAC), and was recently awarded the second place in the Annual IEEE-Venezuela National Competition for the best undergraduate research work.



**Javier A. Salcedo** (S'99–M'99) was born in Mérida, Venezuela, in 1977. He received the electronics engineering degree from the Simón Bolívar University (SBU), Caracas, Venezuela, in 1999. He is currently pursuing graduate studies at the University of Central Florida, Orlando.

After graduation, he worked as an Instructor at the Department of Electronics of SBU, where he also worked on research at the Solid-State Electronics Laboratory. He has coauthored four papers in international journals, three in international conference proceedings and two in local conferences. His research interests include development of compact device models, advanced-physics mechanisms relevant to highly scaled devices and applications thereof to technology, VLSI circuit design, and embedded systems.

Mr. Salcedo is a member of the Venezuelan Association for the Advancement of Science, and the Venezuelan Association of Professional Engineers. His undergraduate senior project was awarded the "Mention of Honor". In 2000, he was a member of the Publications Committee of the "Third IEEE International Caracas Conference on Devices, Circuits and Systems (ICCDCS 2000)," held in Cancún, Mexico, on March 15–17, 2000.