Extraction of the Threshold Voltage of MOSFETs: an Overview

J. J. Liou[1*], A. Ortiz-Conde[2], and F. Garcia Sanchez[2]
[1]Electrical and Computer Engineering Dept.
University of Central Florida, Orlando, Florida, USA
[2]Electronic Engineering Dept.
University of Simon Bolivar, Caracas, Venezuela
[*]Currently with Electrical Engineering Dept.
National University of Singapore, Singapore

Abstract--The threshold voltage is a key parameter in the silicon MOSFET design and operation. This paper gives an overview of the existing methods for extracting the threshold voltage of MOSFETs. In addition, a new extraction method is proposed and developed. Comparisons of the results extracted from the various methods based on device simulation, circuit simulation, and measurements are also presented.

1. INTRODUCTION

The threshold voltage V_T is an important parameter for MOSFET modeling, simulation, and characterization [1-2]. Such a voltage is conventionally defined as the gate voltage that causes the onset of strong inversion in the channel of MOSFETs. Fig. 1 shows a qualitative plot of the inversion layer charge Q'_I vs. the applied gate voltage V_g, which includes the characteristics of depletion, weak inversion, moderate, and strong inversion regions. The point where the Q'_I plot becomes a straight-line is the onset of strong inversion. As seen in Fig. 1, the transition of the exact point toward the straight-line region is very gradual, and no clear point can be identified that could conventionally be taken as the onset of strong inversion. Thus a possible definition of the onset point, which yields V_T, can be the V_g value for which Q'_I is within an acceptable value not much larger than zero. The voltage V_{M0} shown in Fig. 1 fits into this definition. Alternatively, V_T can be determined from the extrapolation of the slope of the linear region, and V_{T0} shown in Fig. 1 would be the appropriate threshold voltage. The last possible definition of V_T is taken at the point where the curve becomes straight-line, which yields $V_T = V_{H0}$. It turns out that V_{H0} is about 0.6 V above V_{M0} at room temperature and for practical fabrication processes [3]. Clearly, the first two definitions have defined the voltage for onset of moderate inversion, whereas the last one has defined the onset for strong inversion. In fact, often no distinction is made between V_{M0}, V_{T0}, and V_{H0} in the literature, and all three are taken to be one and the same point called threshold.

This paper will first review the existing methods for extracting V_T, and a new and improved extraction method will then be developed.

2. EXISTING METHODS FOR EXTRACTING THRESHOLD VOLTAGE

Several methods [1,4-6] have been developed to extract the threshold voltage V_T of a MOSFET biased in the linear region: 1) the constant-current method in which V_T is determined from the gate voltage at a given constant drain current [1]; 2) the linear-extrapolation method which extrapolates the gate voltage axis from the point of maximum slope of the current-voltage characteristics [1]; 3) the second-derivative method in which V_T is determined from taking the second derivative of the drain current I_D with respect to gate voltage V_g (i.e., d^2I_D/dV_g^2) [4]; 4) the ratio method which uses the linear extrapolation of the ratio of the conductance $g = dI_D/dV_D$ and the transconductance $g_m = dI_D/dV_g$ to the gate bias axis [5]; and 5) the quasi-constant-current method which determines V_T from the subthreshold current behavior [6].

The constant-current method is widely used in industry because of its simplicity; the threshold voltage can be determined quickly with only one voltage measurement necessary, as shown in Fig. 2. However, it has the disadvantage of being strongly dependent of the arbitrary choice of current. This is evident by Fig. 3, where different gate voltages at different drain currents are taken to be the threshold voltage.

The linear-extrapolation method is the most extensively employed by researchers, but it presents

the disadvantage of being dependent of the series resistances of the MOSFET. Since I_D vs. V_g curve deviates from a straight line at gate voltage above V_T due to series resistance and mobility degradation effects, it is common practice to find the point of maximum slope by a maximum in the transconductance g_m, fit a straight line to the curve at that point, and extrapolate to $I_D = 0$, as illustrated in Fig. 4.

The second-derivative method [4], developed to avoid the dependence on the series resistances, determines V_T from the peak of $dg_m/dV_g = d^2I_D/dV_g^2$, which is denoted by $V_T(TC)$ in Fig. 5. Also shown in the figure are the threshold voltages extracted from line extrapolation (i.e., $V_T(LE)$) and from the classical definition of surface potential equals twice the bulk potentials (i.e., $V_T(2\phi_F)$). Such a method is highly sensitive to noise in the measurements, however, because the second derivative is equivalent to a high pass filter.

The ratio method [5], developed also to avoid the dependence on the series resistances, suggested that the ratio $g/g_m^{0.5}$ is a linear function of gate bias, whose intercept equals the threshold voltage. Fig. 6 shows the measured $g/g_m^{0.5}$ versus the gate voltage for several n-channel MOSFETs. According to the method, the interception of $g/g_m^{0.5}$ lines of MOSFETs with different channel lengths (i.e., 0.75, 0.875, 1.25 μm shown in Fig. 6) yields the threshold voltage. The main drawback of such a method is the fact that the lines do not necessarily intercept at one point, as clearly shown in Fig. 6. The method also requires extra steps of finding the conductance and transconductance of the MOSFET.

The quasi-constant-current method [6] was derived based on the drain current equation in the subthreshold region. It defines V_T as the gate voltage required for the surface band bending equals twice the bulk potential. In addition to its complexity, such a method is valid only for the subthreshold region, where the electrical characteristic is not as well defined as the strong inversion region.

3. NEW THRESHOLD VOLTAGE EXTRACTION METHOD

A parameter-extraction method has been reported recently [7-9] to eliminate the effect of the series resistances in an arbitrary two-terminal device which contains linear (resistors) and non-linear elements. It was developed based on a new function D, which contains only integrations of current and voltage. The integration acts as a low-pass filter, thus reducing the possibility of measurement errors associated with the extraction procedure. Using the same concept, we present in this section a new method to extract the threshold voltage of the four-terminal MOSFET. The method will be tested in circuit simulator AIM-SPICE [10], device simulator MEDICI [11], and measurements. The results obtained from the new method will also be compared with those obtained from the existing methods.

3.1 Review of the Integral Function for Two-Terminal Devices

For the purpose of extracting the model parameters of a two-terminal device (i.e., p/n junction diode), it would be convenient to use a function that, in addition to being easy to calculate from the device's experimentally measured I-V characteristics, does not depend on the parasitic series resistance. A possible such function can be can be defined by an integral function D [8-9]:

$$D(V,I) \triangleq \int_0^I V\,dI - \int_0^V I\,dV \tag{1}$$

where the first and second terms on the right-hand-side are the device's content and the co-content, respectively, and V and I are the device terminal voltage and current, respectively. The integral function D can also be considered as a measure of the device non-linearity, which would be zero for a device with only linear elements because the content and co-content are identical for such a device.

An arbitrary two-terminal device with both linear and nonlinear elements has the following properties [9]: (a) the summation of the contents over all the branches is zero; and (b) the summation of the co-contents over all the branches is zero. Therefore, the summation of the function D over all the branches is zero. In others words, the function D eliminates the effect of the linear elements, such as series resistances, and can be used for extracting intrinsic parameters of semiconductor devices.

3.2 MOSFET Extraction Method Based on Integral Function

The concept of the integral function used in the two-terminal device parameter extraction is also applicable for three- and four-terminal devices. For the case of a MOSFET biased in the linear region, the drain current can be expressed as:

$$I_D = f(V_{GS} - V_T)V_{DS} \tag{2}$$

where f is a function defined by a particular MOSFET model, and V_{GS} and V_{DS} are the intrinsic gate-source and drain-source voltages, respectively. The two voltages can be related to the external voltages as

$$V_{GS} = V_g - I_D R_s \tag{3}$$

and

$$V_{DS} = V_d - I_D(R_s + R_d) \tag{4}$$

Here V_g and V_d are the extrinsic gate-source and drain-source voltages, respectively, and R_s and R_d are the source and drain series resistances, respectively, which are assumed independent of the gate voltage.

Next, we introduce a change of variable from V_g to V_{gb}, and the reason of using such a new variable will be given later. It is defined as

$$V_{gb} \triangleq V_{\max} - V_g \tag{5}$$

where V_{max} is a constant parameter, which physically represents the maximum gate voltage under consideration (V_{max} = 5 V in our case). In deriving the integral function D_{MOS} for the MOSFET, the variable I used in (1) will be changed to a new variable $(R_m V_{gb})$. This is because (1) was derived based on the property that the series resistance R of a two-terminal device, such as a junction diode, depends linearly on I. For the MOSFET, however, R_d and R_s are assumed constant with respect to I_D, but they depend linearly on the variable $(R_m V_{gb})$. As a result, D_{MOS} can be expressed in terms of V_{gb} and $(R_m V_{gb})$ as

$$D_{MOS}(V_{gb}, R_m V_{gb}) = \int_0^{(R_m V_{gb})} V_{gb}\, d(R_m V_{gb}) - \int_0^{V_{gb}} (R_m V_{gb})\, dV_{gb} \tag{6}$$

Putting (1) into (6), and after some algebraic manipulations, we obtain

$$D_{MOS}(V_{gb}, R_m V_{gb}) = \frac{2V_{gb}}{K} + \frac{V_{gb}^2}{K(V_{\max} - V_{gb} - V_T)} + \frac{2\,(V_{\max} - V_T)}{K} \ln\left[1 - \frac{V_{gb}}{(V_{\max} - V_T)}\right] \tag{7}$$

where K is related to the MOSFET width, MOSFET length, μ_0, and oxide capacitance.

The value of D_{MOS} as a function of V_{gb} can be found by putting the measured or simulated current-voltage data into (1). This, together with the information of K and V_{max}, allows one to determine V_T from (7). It should be mentioned that choosing different V_{max} values does not alter the outcome of V_T.

From the mathematical point of view, we can use V_g instead of V_{gb} in deriving (7), but R_m, and thus D_{MOS}, is very large for small V_g (i.e., weak inversion). Consequently, in the D_{MOS} versus V_g plot, D_{MOS} is very large in a narrow range of small V_g and is small in the remaining range of large V_g (i.e., strong inversion), which makes the fitting to the D_{MOS} versus V_g plot very difficult. This problem can be eliminated by using the variable V_{gb}, which results in a more desirable plot with small D_{MOS} in the weak inversion region and large D_{MOS} in the wider region of strong inversion.

3.3 Circuit Simulation Results

We first simulate an n-channel MOSFET using AIM-SPICE simulator [10] and extract V_T from the SPICE simulation results. The level-3 MOSFET model in SPICE is used in simulation, and the following parameters are used: a threshold voltage of 0.5 V, a mask channel width of 10 μm, a mask channel length of 0.5 μm, a junction depth of 0.10 μm with a lateral extent of 0.075 μm, an oxide thickness of 100 Å, a substrate doping of 10^{17} cm^{-3}, a mobility of 331.5 cm^2/V-s, a bulk threshold parameter of 0.53 $V^{1/2}$, a mobility degradation factor of 0.8 V^{-1}, and a maximum drift velocity for carriers of 10^5 m/s. An increment of 50 mV for the gate voltage and V_d = 50 mV were used in the simulation.

Figure 7(a) shows the drain current as a function of the gate bias simulated for various cases of $R_d = R_s$, and Fig. 7(b) shows the corresponding D_{MOS} as a function of V_{gb}. Clearly, D_{MOS} is independent of the drain and source series resistances.

Figure 8 shows the threshold voltages as a function of $R_d = R_s$ extracted from the different methods based on the SPICE simulation results. It can be seen that (a) the present method yields the best result of V_T = 0.44 V for all drain and source series resistances (i.e., closest to V_T = 0.5 V specified in simulation); (b) the linear-extrapolation method is highly dependent of the series resistances; (c) the second-derivative method becomes insensitive to the series resistances for $R_d = R_s > 10$ KΩ; and (d) the ratio method depends only slightly on the series resistances but has the largest error among all methods considered.

3.4 Device Simulation Results

Here, a two-dimensional device simulator MEDICI [11] is used, and p-channel LDD MOSFETs with a mask channel length L_m = 0.75 μm and typical device make-up [12] are simulated.

Figure 9(a) presents the drain current as a function of the gate bias simulated for a fixed drain contact resistance R_{cd} = 1 KΩ-μm and several different source contact resistances R_{cs}. The reason of using R_{cd} and R_{cs} here, rather than R_d and R_s, is because only the drain and source contact resistances, not the drain and source series resistances, can be specified in device simulation. Also note that R_{cd} and R_{cs} are part of R_d and R_s, respectively. Figure 9(b) shows D_{MOS} as a function of V_{gb} calculated from the simulation results in Figure 9(a). We observe that the function D_{MOS} is independent of the contact resistances.

Fig. 10 shows the threshold voltages as a function of R_{cs} extracted from the various methods based on the MEDICI simulation results. The trends are similar to those obtained from SPICE simulation shown in Fig. 8. First, the constant-current method is insensitive to R_{cs} and yields the smallest V_T for a wide range of R_{cs} (i.e., $R_{cs} < 5$ KΩ-μm). Second, both the linear-extrapolation and second-derivative methods depend strongly on R_{cs}. Third, among all methods considered, the present method is the least sensitive to R_{cs}. However, some discrepancies between Figs. 8 and 10 can be found, such as the different tendencies of the second-derivative and ratio methods obtained from SPICE and MEDICI simulations. This is due to the different types of resistances used in Figs. 9 and 10 and, to a less extent, different mobility models used in SPICE and MEDICI simulations.

3.5 Measurements

The drain current versus the gate voltage characteristics measured from a 2-μm MOSFET are presented in Fig. 11(a). An increment of 100 mV for the gate voltage and V_d = 100 mV have been used in the measurement. Figure 11(b) shows the corresponding D_{MOS} as a function of V_{gb}.

Table 1 shows the threshold voltages extracted from the various methods. The results show that the constant-current and second-derivative methods give the smallest and largest V_T, respectively, and that the present and linear-extrapolation methods yield comparable V_T. This trend is in good agreement with that obtained from MEDICI simulation shown in Fig. 10.

4. CONCLUSION

Various methods reported in the literature for extracting the threshold voltage of MOSFETs have been reviewed, and their advantages and disadvantages discussed. A new and improved extraction method has also been developed and presented, which was shown to be independent of the drain and source resistances and more accurate than the existing extraction methods.

REFERENCES

[1] D. K. Schroeder, *Semiconductor Material and Device Characterization*, Wiley, New York, 1990.

[2] J. J. Liou, *Advanced Semiconductor Device Physics and Modeling*, Artech House, Inc., Boston, (1994).

[3] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*, New York: McGraw-Hill, 1987.

[4] H. S. Wong, M. H. White, T. J. Krutsick and R. V. Booth, "Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFET's," Solid-St. Electron., 30, 953, (1987).

[5] S. Jain, "Measurement of threshold voltage and channel length of submicron MOSFETs," IEE Proc. Cir. Dev. and Sys., 135, 162, (1988).

[6] Z. X. Yan and M. J. Deen, "Physically-based method for measuring the threshold voltage of MOSFETs," IEE Proc. Cir. Dev. and Sys., 138, 351, (1991).

[7] A. Ortiz-Conde, F. J. García Sánchez, J. J. Liou, J. Andrian, R. J. Laurence, and P. E. Schmidt, Solid-St. Electron., 38, 265, (1995).

[8] F. J. García Sánchez, A. Ortiz-Conde, and J. J. Liou, IEE Proc. Cir. Dev. and Sys., 143, 68, (1996).

[9] F. J. García Sánchez, A. Ortiz-Conde, G. De Mercato, J. J. Liou, and L. Recht, IEEE Int. Caracas Conf. on Dev. Cir. and Sys., (Caracas, Venezuela), 1, 298, (1995).

[10] K. Lee, M. Shur, T. A. Fjeldly, and T. Ytterdal, *Semiconductor Device Modeling for VLSI*, Prentice-Hall, Englewood Cliffs, 1993.

[11] MEDICI Manual, Technology Modeling Associates, Inc. (1993).

[12] Md. Rofiqul Hassan, J. J. Liou, A. Ortiz-Conde, F. J. García Sánchez, and E. Gouveia Fernandes, Solid-St. Electron., in press (1996).

Table 1
Extracted threshold voltages using experimental data

Method	Threshold voltage For W/L= 20/2
Constant current @ 100 nA	0.657
Linear extrapolation [1]	0.889
Second derivative [4]	1.000
Ratio of conductance and transconductance [5]	0.873
Integral function (present method)	0.909

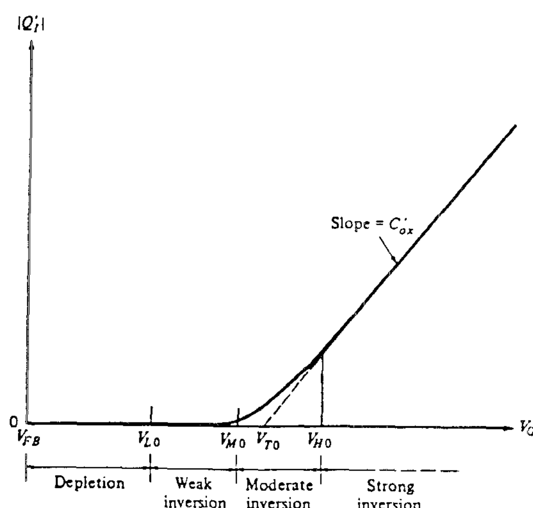


Fig. 1 Qualitative plot of inversion layer charge vs gate voltage.

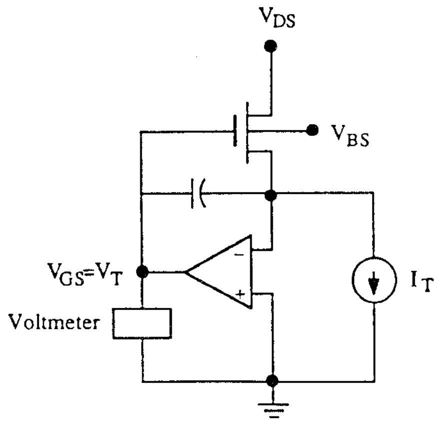


Fig. 2 Measurement setup for the constant current threshold voltage method.

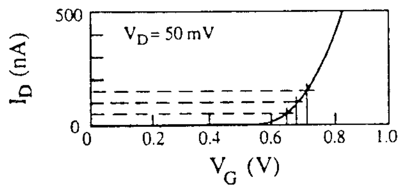


Fig. 3 Qualitative plot to illustrate the different threshold voltages determined from different drain currents.

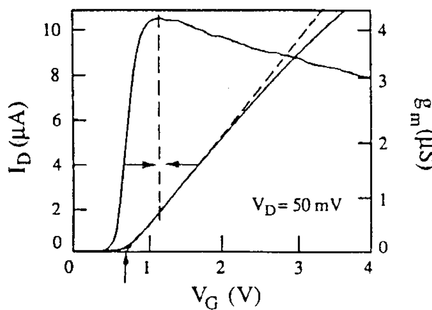


Fig. 4 Plots of drain current and transconductance to illustrate the linear extrapolation threshold voltage method.

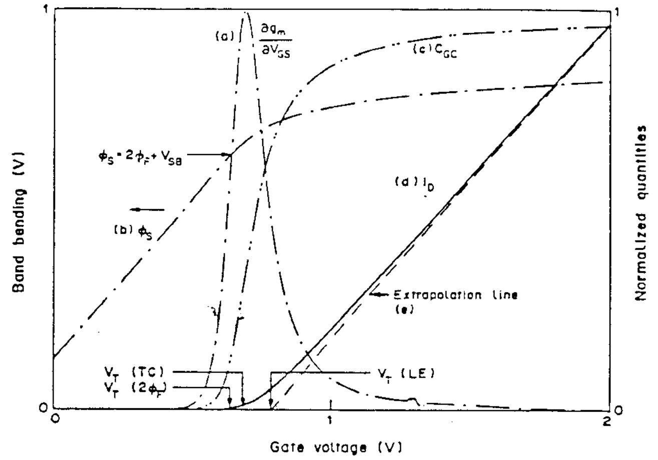


Fig. 5 Schematic illustration of determining the threshold voltage from the second-derivative method (i.e., V_T(TC)), from the line extrapolation method (i.e., V_T(LE)), and from the classical method of surface potential equals twice the bulk potential (i.e., $V_T(2\phi_F)$).

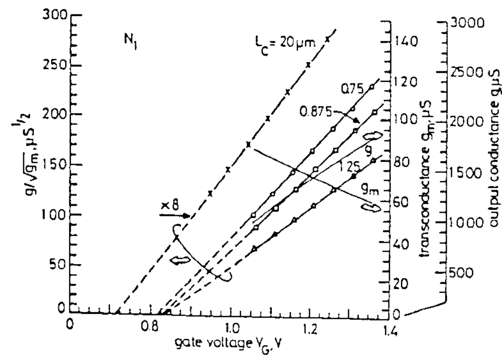
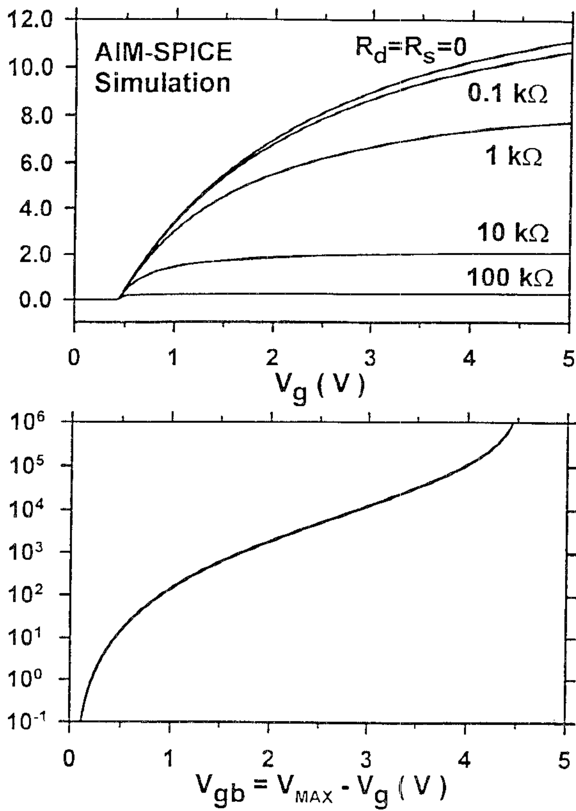


Fig. 6 Measured $g/g_m^{0.5}$ as a function of the gate voltage. The interception of the lines at the x-axis yields the threshold voltage.



(a)

(b)

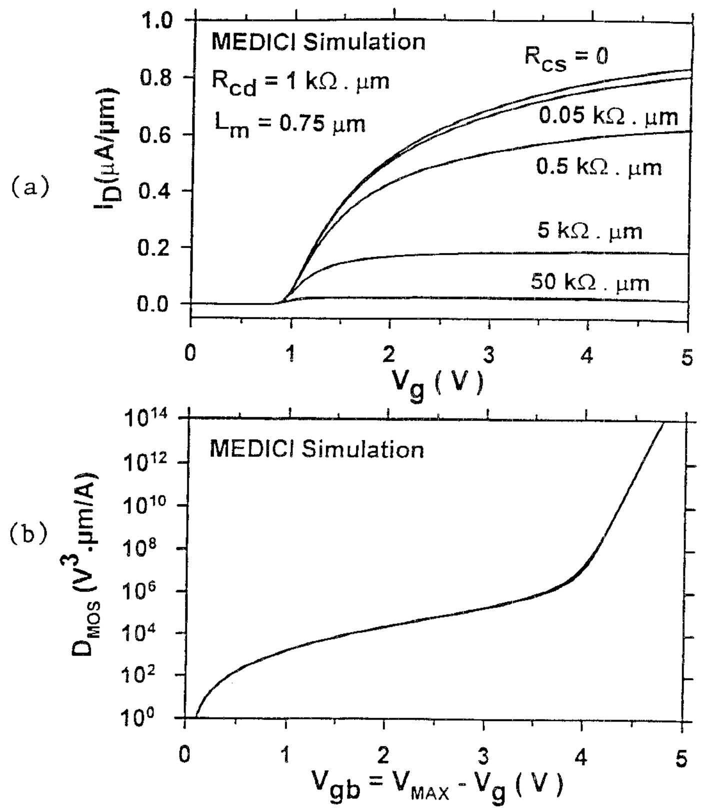


Fig. 7 (a) Drain current versus gate voltage characteristics and (b) corresponding D_{MOS} function simulated using AIM-SPICE for different drain and source series resistances.

Fig. 9 (a) Drain current versus gate voltage characteristics and (b) corresponding D_{MOS} function simulated using MEDICI for different contact resistances.

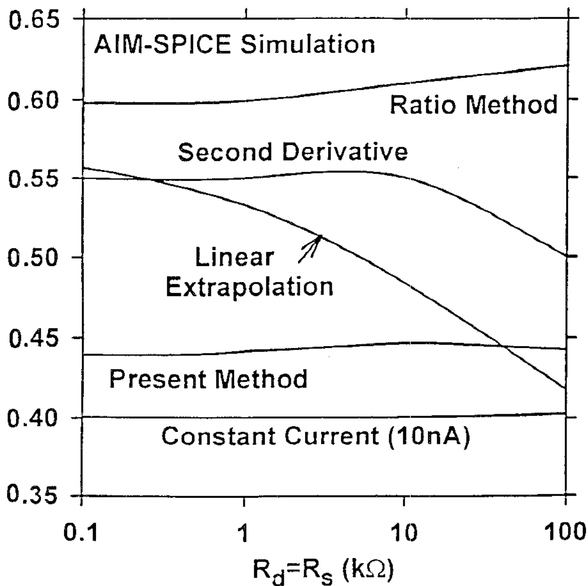


Fig. 8 Comparison of threshold voltages extracted using the different methods based on the results of SPICE simulation.

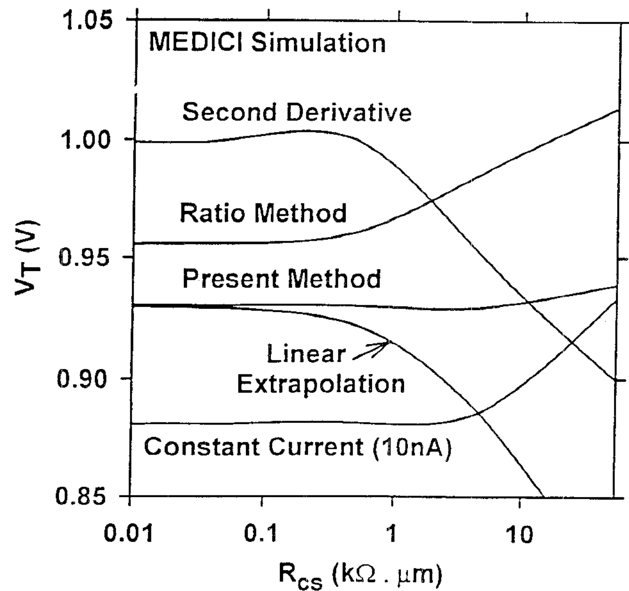


Fig. 10 Comparison of threshold voltages extracted using the different methods for based on the results of MEDICI simulation.

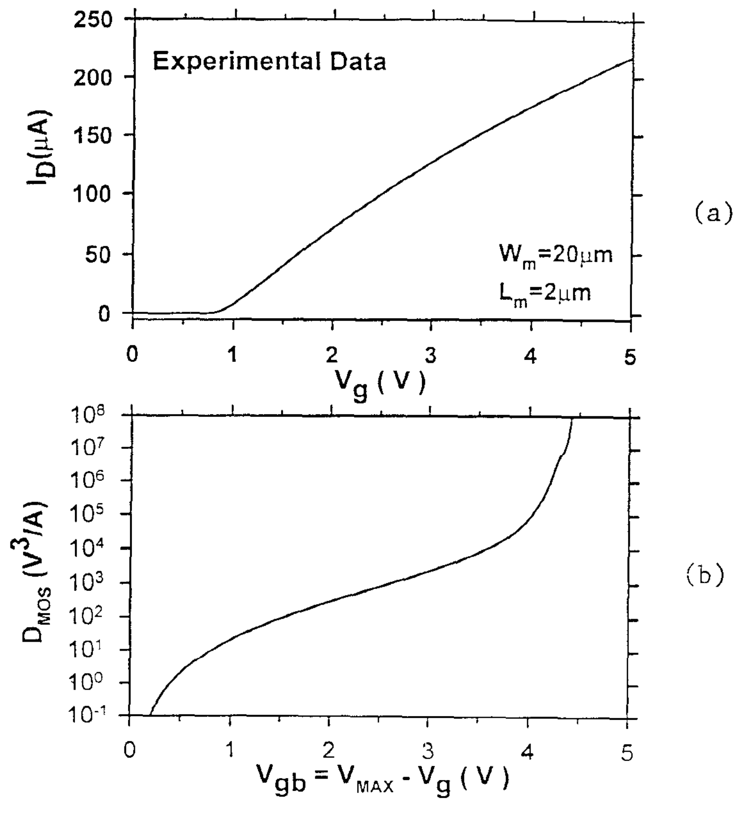


Fig. 11 (a) Drain current versus gate voltage characteristics and (b) corresponding D_{MOS} function obtained from measurements.