



Modeling real junctions by a series combination of two ideal diodes with parallel resistance and its parameter extraction

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Abstract

A technique is proposed to extract the reverse saturation current parameter and ideality factor of semiconductor junctions from the low forward voltage region of the device's characteristics, even under the presence of significant parallel resistance effects. The series combination of two ideal diodes is proposed for modeling real devices with a non-linear contact resistance, in which case, the effective ideality factor at high voltage is higher than that of low voltage. It is proved, under certain physical assumptions, that the series combination of two ideal diodes can be modeled as a single effective diode for low voltage and another effective diode for high voltage. Both techniques were tested and their accuracy verified on experimental and simulated I – V characteristics. © 2001 Published by Elsevier Science Ltd.

Keywords: Non-ideal diode; Approximate diode model; Diode ideality factor; Diode reverse saturation current

1. Introduction

The current voltage characteristics of real diodes may be modeled by a modified single exponential Shockley expression [1]:

$$I = I_0 \left[\exp\left(\frac{V}{nV_t}\right) - 1 \right], \quad (1)$$

where the pre-exponential factor I_0 is the reverse saturation current, V is the voltage at the junction, $V_t = kT/q$ is the thermal voltage, and n is the so-called quality or junction ideality factor. The experimentally measured characteristics often present a more complex behavior because of the various conduction mechanisms that may be present. A summation of two (or sometimes more)

exponential expressions, each one of them with different values of reverse current and ideality factors, is frequently used to model the various conduction mechanisms [2]:

$$I = I_{01} \left[\exp\left(\frac{V}{n_1 V_t}\right) - 1 \right] + I_{02} \left[\exp\left(\frac{V}{n_2 V_t}\right) - 1 \right]. \quad (2)$$

It is important to point out that the model described in the previous equation is equivalent to two ideal diodes connected in parallel and the ideality factor at low voltage will be higher than that at high voltage.

The effects of parasitic series and parallel resistances are also frequently significant [1–6] and they can obscure the intrinsic parameters of semiconductor devices. Many methods [7–10] have been presented to extract the parameters of a single-exponential diode with only series resistance from experimental I – V characteristics. However, few methods [4,11] have been reported to extract the parameters of a single-exponential diode having a significant shunt resistance. Not many extraction methods have been reported either for the cases of real diodes

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that require to be modeled with a double exponential [2], and to the best of our knowledge they have not accounted for significant parallel and series resistance.

In the present work we will present a procedure to extract the physical intrinsic device parameters of a semiconductor junction affected by the presence of a non-linear metal–semiconductor contact, as well as parallel and series resistance. The series combination of two ideal diodes will be proposed for modeling real devices with non-linear contact resistance, for which case the effective ideality factor at high voltage turns out to be higher than that at low voltage. Our approach will be based first on extracting two separate models: one for low voltage and another for high voltage. In Section 2, we will describe a method, for the low voltage region, to extract the intrinsic parameters of a single-exponential diode for the case in which the current is dominated by the parallel resistance. For the high voltage range we will use a previously published method [9] to extract parameters of a single-exponential diode with a significant series resistance.

In the experimental diode that we will use the extracted ideality factor at low voltage is smaller than at high voltage, and thus, it cannot be modeled as two ideal diodes connected in parallel. This experimental fact that the ideality factor for low voltage results to be smaller than that at high voltage has been already reported [12]. In Section 3, we will study this series combination of two ideal diodes and we will prove, under certain physical assumptions, that it can be modeled as a single effective diode for low voltage and as another effective diode for high voltage. In Section 4, we compare results from simulations with experimental results. Our method is based on integration in order to reduce the effect of experimental noise during the parameter extraction procedure [9].

2. Parameter extraction in a diode with significant parallel resistance

In this section, we will present a method to extract parameters of a diode for the case in which the current is dominated by the parallel resistance. The present method is based on using the difference integral function (DIF), which is defined as [9]:

$$\text{DIF} \equiv \int_0^I V dI - \int_0^V I dV = IV - 2 \int_0^V I dV, \quad (3)$$

where V is the voltage and I is the current. We will use the function DIF, which has units of power, because it will eliminate the effects of the parallel resistance altogether.

For this case, the I – V characteristics of a real diode may be modeled by the circuit presented in Fig. 1 in

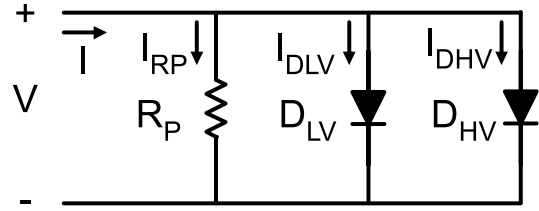


Fig. 1. Lumped circuit model of a double-exponential junction, with parasitic parallel resistance (R_P).

which the ideal diode D_{LV} models the low voltage diode current, the ideal diode D_{HV} describes the high voltage behavior and R_P accounts for a linear parasitic shunt current. Then, the total current is given by:

$$I = I_{OLV} \left[\exp\left(\frac{V}{n_{LV}V_t}\right) - 1 \right] + I_{OHV} \left[\exp\left(\frac{V}{n_{HV}V_t}\right) - 1 \right] + \frac{V}{R_P}, \quad (4)$$

where I_{OLV} and I_{OHV} are the corresponding reverse saturation currents of the diodes, n_{LV} and n_{HV} are the diode ideality factors, and R_P is the parallel resistance. The extraction of the parameters I_{OLV} , I_{OHV} , n_{LV} and n_{HV} is customarily performed either by optimization or by graphical analysis of $\ln(I)$ versus V plots. For the particular case of significant effects due to R_P , the linear portion of $\ln(I)$ versus V could disappear at low voltage, and therefore the determination of I_{OLV} and n_{LV} becomes impossible or unreliable, even using sophisticated optimization fitting procedures. Eliminating the effect of R_P is therefore of paramount importance for the extraction procedure. This is the essence and motivation for using the integral function. Substituting Eq. (4) into the right-hand side of Eq. (3), we obtain:

$$\begin{aligned} \text{DIF} = & I_{OLV} \left[(V - 2n_{LV}V_t) \exp\left(\frac{V}{n_{LV}V_t}\right) + (V + 2n_{LV}V_t) \right] \\ & + I_{OHV} \left[(V - 2n_{HV}V_t) \exp\left(\frac{V}{n_{HV}V_t}\right) + (V + 2n_{HV}V_t) \right]. \end{aligned} \quad (5)$$

It is important to point out that DIF does not depend on R_P at all, as it is indicated in the previous equation. Using the reasonable assumption that the ideal high voltage diode D_{HV} has negligible effect on the low voltage region, Eq. (5) can be approximated by:

$$\begin{aligned} \text{DIF} \approx & I_{OLV} \left[(V - 2n_{LV}V_t) \exp\left(\frac{V}{n_{LV}V_t}\right) \right. \\ & \left. + (V + 2n_{LV}V_t) \right]. \end{aligned} \quad (6)$$

This could represent the case of having highly resistive non-ohmic contact to the diode. The function DIF

for low voltage, obtained by numerical calculation from the experimental data using Eq. (3), contains only two parameters to be extracted: I_{OLV} and n_{LV} . But the direct extraction of these two parameters from the plot of DIF versus V might fail because of the exponential dependence. An alternate procedure consists on assuming a certain reasonable value of n_{LV} and plotting the estimated I_{OLV} versus V obtained from Eq. (6):

$$I_{OLV} = \frac{\text{DIF}}{\left[(V - 2n_{LV}V_t) \exp\left(\frac{V}{n_{LV}V_t}\right) + (V + 2n_{LV}V_t) \right]} \quad (7)$$

If the right value of n_{LV} were used, the plot of the estimated I_{OLV} versus V should be a constant value, which would be the correct value of I_{OLV} .

In order to verify the procedure, we present in Fig. 2 the synthetic I - V characteristics, simulated with AIM-SPICE [13], of a diode having $n_{LV} = 2$, $I_{OLV} = 10^{-10}$ A, $n_{HV} = 1$, $I_{OHV} = 10^{-15}$ A and $R_p = 1$ M Ω . We observe in this figure that: (a) the current in the branch of R_p (I_{RP}) dominates for $V < 0.4$ V; (b) the current passing through D_{HV} (I_{DHV}) dominates for $V > 0.6$ V; and (c) there is not a single region of I which can be approximated by the current going through D_{DLV} (I_{DLV}). Therefore, graphical analysis of $\ln(I)$ versus V would fail to extract n_{LV} and I_{OLV} . An optimization fitting procedure would also fail for this case because I_{DLV} does not approximate the total current at any region of voltage.

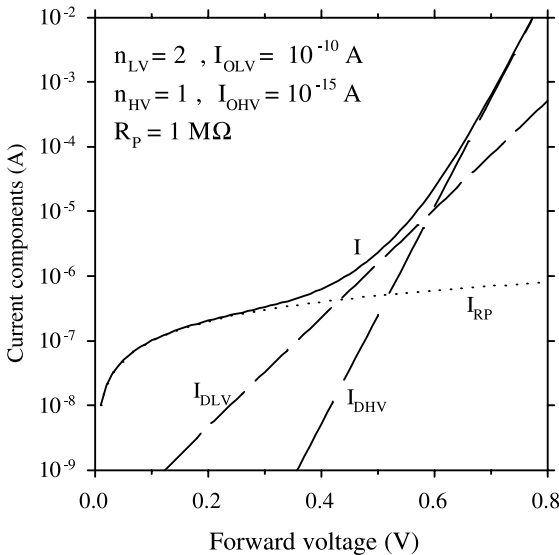


Fig. 2. Synthetic I - V characteristics (I) of a junction simulated by the double exponential expression of Eq. (4) with the parameters indicated. Also shown are the three branch components of the total current: I_{RP} (\cdots), I_{DLV} ($---$) and I_{DHV} ($---$) which correspond to the current through the parallel resistance (R_p), the low voltage diode (D_{LV}) and the high voltage diode (D_{HV}) respectively.

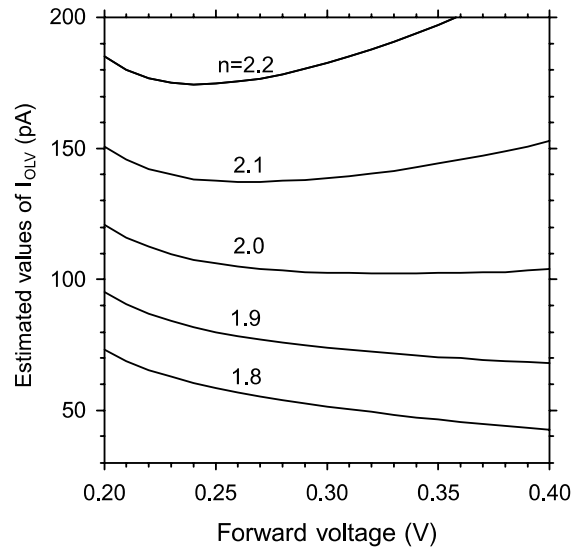


Fig. 3. Estimated values of I_{OLV} obtained by plotting Eq. (7) for the simulated I - V results used in the previous figure and several values of n_{LV} . Note that the plot corresponding to $n_{LV} = 2$ is the closest to be a constant value. Therefore, the extracted value of I_{OLV} is about 10^{-10} A, which correctly corresponds to the value used in the simulation.

Fig. 3 illustrates the results obtained by plotting Eq. (7) for several values of n_{LV} from 1.8 to 2.2 with increments of 0.1. We observe that when $n_{LV} = 2$ the plot of the estimated I_{OLV} versus V is the closest to a constant value. Therefore, our extracted value of I_O is about 10^{-10} A, which corresponds to the correct value used for the simulation.

3. A series combination of two ideal diodes for modeling a real device

Plots of $\ln(I)$ versus V for real devices often present two regions that approach straight-line behavior. For many cases, the slope of the straight line for low voltage is smaller than that at high voltage, implying that the ideality factor at low voltage is higher than that at high voltage. When this condition occurs, the parallel combination of ideal diodes is a good model. However, there are some experimental cases [12] for which the low voltage slope of the straight line is larger than that in the high voltage range, which implies that the ideality factor for low voltage is smaller than that for high voltage. In such cases, the parallel combination of ideal diodes cannot be used as a model. In contrast, we will show that a series combination of ideal diodes represents a good model for this case.

In this section we will prove, under certain physical assumptions, that the series combination of two ideal

diodes can be modeled as a single effective diode for low voltage and another effective diode for high voltage. This particular situation could be caused by the presence of a poor ohmic contact at a semiconductor–metal interface. A real case in which this situation occurs will be presented in Section 4.

The total voltage for the two ideal diodes in series, illustrated in Fig. 4, is given by the summation of the voltages of the individual diodes:

$$V = V_1 + V_2. \quad (8)$$

Substituting the equations for the voltages of each diode,

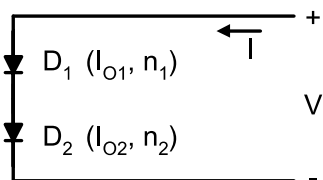
$$\frac{V}{V_t} = n_1 \ln \left(\frac{I}{I_{O1}} + 1 \right) + n_2 \ln \left(\frac{I}{I_{O2}} + 1 \right), \quad (9)$$

where I_{O1} and I_{O2} are the corresponding saturation currents of the diodes, and n_1 and n_2 are the diode ideality factors. Then, taking exponentials in both sides of the previous equation:

$$\exp(V/V_t) = \left(\frac{I}{I_{O1}} + 1 \right)^{n_1} \left(\frac{I}{I_{O2}} + 1 \right)^{n_2}. \quad (10)$$

In the present analysis we will assume that $I_{O1} \ll I_{O2}$. For high currents ($I \gg I_{O2} \gg I_{O1}$) the previous equation can be approximated by

$$\exp(V/V_t) \approx \frac{I^{n_1+n_2}}{I_{O1}^{n_1} I_{O2}^{n_2}} \quad (11)$$



Assuming $I_{O1} \ll I_{O2}$, we obtain the following two equivalent circuits:

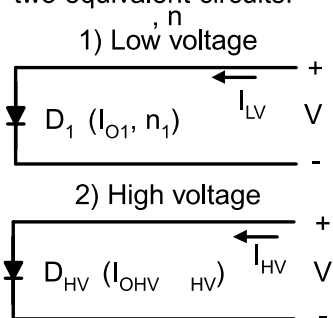


Fig. 4. Lumped circuit model of a double exponential series diode and its equivalent effective low and high voltage diodes.

and solving the current for the high voltage range we obtain:

$$I_{HV} \approx I_{O1}^{n_1/(n_1+n_2)} I_{O2}^{n_2/(n_1+n_2)} \exp \left[\frac{V}{(n_1 + n_2)V_t} \right]. \quad (12)$$

This equation implies that we can model the current, in this region, using a single effective high voltage diode with an ideality factor of

$$n_{HV} \approx n_1 + n_2 \quad (13)$$

and a saturation current of

$$I_{OHV}^{n_{HV}} \approx I_{O1}^{n_1} I_{O2}^{n_2}. \quad (14)$$

For small currents ($I_{O1} \ll I \ll I_{O2}$) which correspond to the low voltage region, Eq. (10) is approximated by:

$$\exp(V/V_t) = \left(\frac{I}{I_{O1}} \right)^{n_1}, \quad (15)$$

and solving the current for the low voltage region we obtain:

$$I_{LV} \approx I_{O1} \exp(V/V_t) \quad (16)$$

which implies that the diode D_1 is controlling the I – V characteristics for this region.

The intersection point of these currents, resulting from the low voltage and the high voltage effective diodes, defines the borderline voltage, V_B , at which point both diodes are comparably important. Using Eqs. (12)–(14) and (16), we obtain:

$$V_B \approx \frac{V_t \ln \left(\frac{I_{OHV}}{I_{O1}} \right)}{\frac{1}{n_1} - \frac{1}{n_{HV}}}. \quad (17)$$

In order to illustrate the present ideas, we show in Fig. 5 the simulated I – V characteristics of a two series diode connection (solid lines) with $n_1 = 1$, $I_{O1} = 10^{-15}$ A and $n_2 = 2$, $I_{O2} = 10^{-10}$ A. We also present in this figure the current for the equivalent low voltage diode (dotted line) with $n_{LV} = 1$, $I_{OLV} = 10^{-15}$ A and for the high voltage diode (short dashed line) having $n_{HV} = 3$, $I_{OHV} = 2.15 \times 10^{-12}$ A. It is shown in this figure that the current of the two diodes in series is well approximated by I_{LV} , in the low voltage region, and by I_{HV} for the high voltage region.

4. Parameter extraction from measurements

Fig. 6 shows the measured I – V characteristic (using symbols) of a hydrogenated amorphous silicon p-i-n diode fabricated following the procedure described in [14]. The data was taken, at room temperature, using a Keithley test system with a voltage step of 10 mV. This figure also presents the simulated results using the parameters that will be extracted in this section.

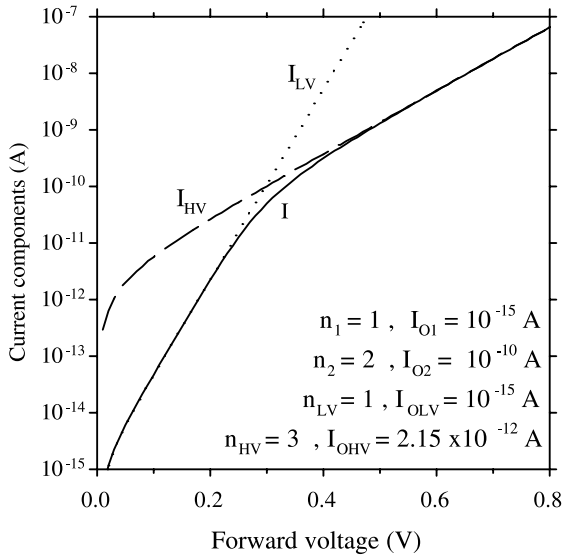


Fig. 5. Synthetic I - V characteristics (labeled I) of a two-diode series connection with ideality factors and reverse currents as indicated. The currents for the two effective diodes and their respective parameters are also shown: I_{LV} (\cdots) and I_{HV} ($-\cdots-$) corresponding to the low and high voltage regions respectively.

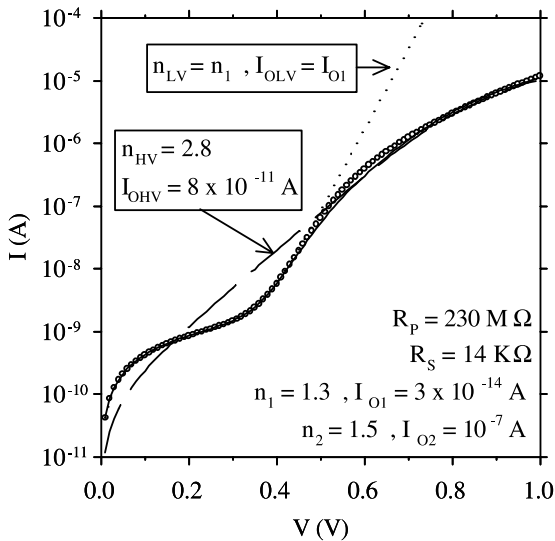


Fig. 6. Experimental I - V characteristics (\circ) of a hydrogenated amorphous silicon p-i-n diode measured with a voltage step of 10 mV. It is obvious that the series resistance is very important at high voltage and that the parallel resistance is dominant at low voltage. The I - V characteristics (continuous line) simulated using the series combination model with the extracted parameters indicated is also shown. Additionally, both approximations (effective diodes), corresponding to the low (\cdots) and high voltage regions ($-\cdots-$), are also included.

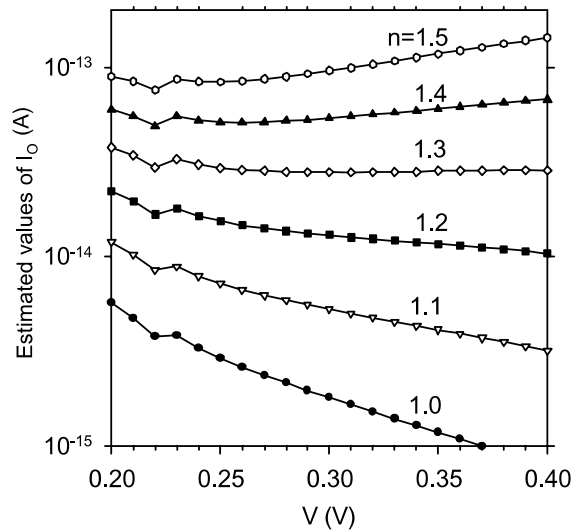


Fig. 7. Estimated values of I_{OLV} obtained by plotting Eq. (7) for the experimental I - V results presented in the previous figure and several values of n_{LV} . We observe that for $I_{OLV} = 1.3$ the plot of the estimated I_{OLV} versus V is the closest to a constant value; therefore we conclude that the extracted value of I_{OLV} is 3×10^{-14} A.

Our approach to model this device is based on first extracting two separate models: one for the low voltage region and another for the high voltage region. Later, the two models will be joined. We observe that the current is proportional to the voltage for $V < 0.3$ V; therefore, a parasitic parallel resistance dominates in this region and its extracted value is $R_p = 230$ M Ω . The problem for the low voltage region is the extraction of the diode's intrinsic parameters which are obscured by the presence of that parallel resistance. Using the extraction technique described in Section 2, we present in Fig. 7 the estimated I_{OLV} versus V obtained by plotting Eq. (7), for values of n_{LV} from 1.0 to 1.5 with increments of 0.1, in the voltage range from 0.2 to 0.4 V. We find that the plot corresponding to for $n_{LV} = 1.3$ is the closest to a constant value; therefore, the extracted value of I_{OLV} is taken to be 3×10^{-14} A.

For the high voltage ($V > 0.6$ V) the series resistance becomes very important and the plot of $\ln(I)$ vs. V starts to deviate from a straight line. The derivative of the voltage with respect to the current at $V = 1$ V, is 15 k Ω ; which implies that R_s should be smaller than this value. The problem for the high voltage region is the extraction of the diode's parameter which are obscured by this series resistance. Following a previously published method [9,15] for this region we obtain: $n_{HV} = 2.8$, $I_{OHV} = 8 \times 10^{-11}$ A and $R_s = 14$ k Ω .

It is important to point out that in this case the parallel combination of ideal diodes cannot be used as a model because $n_{HV} > n_{LV}$. We will use the series

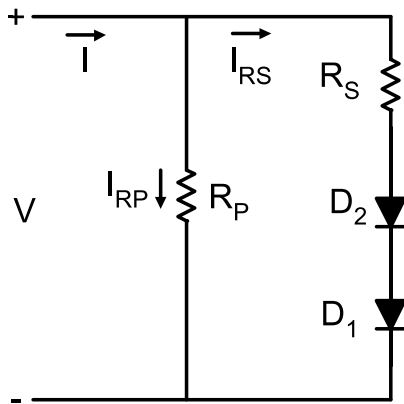


Fig. 8. Lumped circuit model of a double exponential series diode, with parasitic series resistance (R_S) and parasitic parallel resistances (R_P).

combination of two ideal diodes, as mentioned before, with series and parallel resistance as illustrated in Fig. 8. Using Eqs. (13) and (14) and the fact that the diode D_1 is controlling the I - V characteristics for low voltages, we obtain: $n_1 = 1.3$, $I_{O1} = 3 \times 10^{-14}$ A, $n_2 = 1.5$ and $I_{O2} = 10^{-7}$ A. Fig. 6 also presents the simulated total current (solid line) which approximates very well the experimental data. In order to illustrate the behavior of both approximations for the low and the high voltage regions, Fig. 6 also shows: (a) the simulated current of the low voltage diode (D_{LV}) in parallel with R_P (dotted line), and (b) the current of the high voltage diode (D_{HV}) in series with R_S (dashed line). Both approximations are very good in their corresponding regions and they intersect at the borderline voltage of 0.5 V which is in agreement with Eq. (17). It is worth mentioning that direct optimization, which was implemented in an S-Plus [16] environment, failed to extract the parameters for this device because the diode parameters are extremely obscured by the parasitic series and shunt resistances.

5. Conclusions

We have presented a technique to extract the intrinsic parameters of semiconductor junctions which are obscured by the presence of significant effects of a parasitic resistances. The series combination of two ideal diodes is also proposed for modeling real devices in which the ideality factor at high voltage is higher than that for the low voltage region. It is proved that the series combination of two ideal diodes can be modeled as a single effective diode for the low voltage region and another effective diode for high voltage. Both technique have been tested and their accuracy verified on experimental and simulated I - V characteristics.

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