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New method for determination of harmonic distortion in SOI FD transistors

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Abstract

We present a new method for calculating the total harmonic distortion (THD) and the third harmonic distortion (HD3) of the output current–voltage characteristics of a semiconductor device. The method is based on the calculation of two functions which we call *D* and *D*3 and are based on a specific integration of the DC current–voltage characteristic of the device.

In this paper we demonstrate that function *D* can be correlated with the THD and function *D*3 with the HD3, so that they can be determined in a much simpler way, with no need to use derivatives, Fourier coefficients or fast Fourier transforms.

The new method is applied to calculate the harmonic distortion of a silicon-on-insulator (SOI) fully depleted (FD) MOS transistor in the triode regime to be used as an active resistor at the input of an operational amplifier in a MOSFET-C filter configuration.

It is also demonstrated that the transistor I_{DS}–V_{DS} characteristics used in these calculations can be obtained from either measurements, analytical models or numerical simulations. © 2002 Elsevier Science Ltd. All rights reserved.

1. Introduction

The harmonic distortion introduced by MOS transistors is a property of major importance regarding their analog applications [1]. In particular, in MOSFET-C continuous-time filter architectures, MOS transistors can be used, in triode regime, as linear resistors at the input of operational amplifiers [2–5]. In such balanced or fully differential implementations, the total harmonic distortion (THD) is dominated by its third-order component (third harmonic distortion, HD3). Up to now, methods used to calculate the THD and DH3 were based on the use of the fast Fourier transform (FFT), or on the calculation of high-order derivatives of the output characteristic [1], and very often on uneasy AC measurements [4]. A five points method applied to a current mirror circuits was also used in Ref. [6]. In this work we present a new method to calculate the THD and the HD3 of MOS transistors used as linear resistors, which is based on the direct analysis of the non-linearity of the DC I_{DS}–V_{DS} characteristics of the device for a fixed gate voltage. To evaluate this non-linearity, we use a function *D* which was first defined and presented in Ref. [7] as an integral equation of the I_{DS}–V_{DS} characteristic. The use of this function has the advantage of noise reduction when processing experimental data and has been used for the extraction of other device parameters, as for example Ref. [8].

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In this paper, in order to eliminate the even harmonics, we further introduce another function, which we call $D3$. It is demonstrated that the function D can be correlated with the THD and function $D3$ with the HD3, so that THD and HD3 can be determined in a much simpler way, with no need to use high-order derivatives, Fourier coefficients (FC) or a FFTs.

The method is applied to silicon-on-insulator (SOI) fully depleted (FD) MOSFETs which were previously demonstrated to feature, when used as linear resistors in their triode regime, much lower harmonic distortion than bulk Si equivalents [4,5]. Their I_{DS}–V_{DS} characteristics were measured in the region of interest with fixed gate bias and variable drain voltage. The devices were also simulated numerically (using ATHENAS and ATLAS 2D coupled process/device simulators) [1] as well as modeled and calculated through an analytical expression.

2. I_{DS}–V_{DS} characteristic

The following I_{DS}–V_{DS} model of the SOI FD MOSFET in the triode region, for zero substrate bias, strong inversion and a depleted back interface from source to drain, was derived from [9].

$$I_{DS}(V_{DS}) = \frac{K_0\left(V_{GT}V_{DS} - \frac{(1+\alpha)}{2}V_{DS}^2\right)}{1 + \theta_G V_{GT} + \theta_D V_{DS}}, \quad (1)$$

where

$$K_0 = \frac{W}{L}\mu_0 C_{01}, \quad (2)$$

$$V_{GT} = V_{GS} - V_T, \quad (3)$$

$$\alpha = \frac{C_{02}C_S}{C_{01}(C_S + C_{02})}, \quad (4)$$

W denotes the channel width, L, the channel length, V_T, the threshold voltage, C_S, the silicon film capacitance, C_{01}, the front gate capacitance, C_{02}, the back gate capacitance, θ_G and θ_D, the mobility field dependent parameters, including the effect of the series resistance. In this paper θ_G and θ_D are used as adjustment parameters for the semi-empirical Eq. (1).

The transistors under study have a gate oxide thickness of 30 nm, a silicon thickness of 80 nm, a back oxide thickness of 400 nm and $\alpha = 0.07$. The channel width is 20 μm and the channel lengths 2 and 20 μm. The I_{DS}–V_{DS} characteristic were measured as well as simulated using coupled 2D process/device technological simulations.

Table 1
Extracted parameters for $V_{GS} = 1.5$ V and $V_{BS} = 0$ V

L (μm)	K_0 (A/V^2)	V_T (V)	θ_G (1/V)	θ_D (1/V)
2	5.93×10^{-4}	0.37	0.056	−0.048
20	6.2×10^{-5}	0.38	0.025	−0.024

The parameters extracted to fit Eq. (1) on the measurements are given in Table 1. The measured, simulated and analytical I_{DS}–V_{DS} curves are shown in Fig. 1 for $V_{GS} = 1.5$ V, where V_{DS} plotted along the X-axis goes from a maximum negative $-V_m$ to a maximum positive value, V_m, defining the amplitude of the sinusoidal voltage applied to the drain such as in a MOSFET-C structure. As can be seen, the calculated and simulated I_{DS}–V_{DS} curves have both an excellent agreement, better than 2% with the experimental curve.

3. Definition of function D

In Fig. 1 it is clear that the I_{DS}–V_{DS} characteristic is not completely linear, and this deviation from linearity can give us a criterion of the distortion introduced by this device for an input sinusoidal signal superposed to the drain. Applying the integration method presented in Ref. [7] we can use the function D defined as the difference of areas above and below the I_{DS}–V_{DS} curve to evaluate the THD. If the I_{DS}–V_{DS} characteristic is linear, function $D = 0$. As soon as non-linearity appears in the curve, D will no longer be equal to zero, and its value will increase as the non-linearity is larger.

We will normalize the current and voltage on Y and X axes respectively, so the I_{DS}–V_{DS} curve shown in Fig. 1

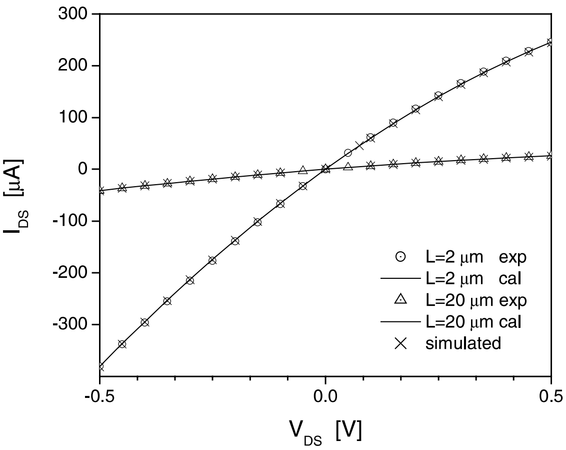

Fig. 1. Measured (⊙ and △), calculated using Eq. (1) with parameters of Table 1 and simulated with ATLAS (×) I_{DS}–V_{DS} characteristics for 2 and 20 μm long SOI FD MOSFETs for $V_{GS} = 1.5$ V at the triode operation region as linear resistor.

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[1] ATLAS and ATHENA are programs of Silvaco International.

is moved into the first quadrant of the graphical representation in order to deal only with positive values of the variables in the interval from 0 to 1, which provide dealing only with positive numbers when integrating the area under the curve in any segment.

The normalized variables can be expressed as:

$$i = \frac{I_{\mathrm{DS}}(V_{\mathrm{DS}}) - I_{\mathrm{DS}}(-V_{\mathrm{m}})}{I_{\mathrm{DS}}(V_{\mathrm{m}}) - I_{\mathrm{DS}}(-V_{\mathrm{m}})}, \tag{5}$$

$$v = \frac{V_{\mathrm{DS}} + V_{\mathrm{m}}}{2V_{\mathrm{m}}}. \tag{6}$$

The analytical normalized current $i(v)$ as a function of the normalized voltage v resulting from Eq. (1) is:

$$i(v) = \frac{1}{2}\frac{(1+P)(1+\gamma)}{(1+P\gamma)}\left[1 - \frac{1 - 2\frac{1+2P}{1+P}v + \frac{4P}{1+P}v^2}{1 + \frac{2\gamma}{1-\gamma}v}\right], \tag{7}$$

where

$$P = \frac{1+\alpha}{2}\frac{V_{\mathrm{m}}}{V_{\mathrm{GT}}}, \tag{8}$$

$$\gamma = \frac{\theta_{\mathrm{D}} V_{\mathrm{m}}}{1 + \theta_{\mathrm{G}} V_{\mathrm{GT}}}. \tag{9}$$

The normalized i–v curves are shown in Fig. 2 indicating the excellent correlation between the analytical model of Eq. (7) and the experimental data normalized using Eq. (5).

Function D is then defined as:

$$D = \int_0^1 i(v)\,\mathrm{d}v - \int_0^1 v(i)\,\mathrm{d}i = 2\int_0^1 i(v)\,\mathrm{d}v - 1. \tag{10}$$

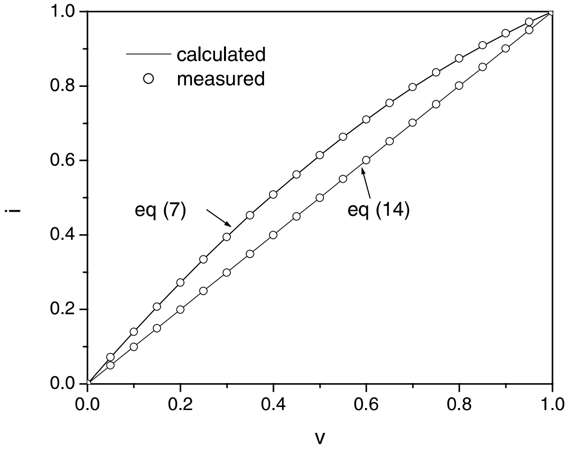

Fig. 2. Normalized current–voltage characteristic calculated from the analytical Eqs. (7) and (14) and from measured data using Eqs. (5) and (6), in the case of a SOI FD MOSFET with $L = 20$ μm, $V_{\mathrm{GS}} = 1.5$ V.

The analytical solution of Eq. (10), using Eq. (7) is equal to:

$$D_{\mathrm{ana}} = \frac{\gamma + P}{2\gamma^3(1+P\gamma)}\left[2\gamma + \left(1-\gamma^2\right)\ln\left(\frac{1-\gamma}{1+\gamma}\right)\right]. \tag{11}$$

For the limiting case when θ_{D} tends to 0, γ also tends to 0 and D_{ana} depends only on the applied voltages and simplifies to:

$$D_{\mathrm{ana0}} = \frac{2}{3}P. \tag{12}$$

4. Definition of function *D*3

Even though the magnitude of HD3 is usually several orders of magnitude below the THD, HD3 becomes dominant in balanced or fully differential circuit designs which suppress the even-order non-linearities. For that reason, to calculate it in our method, we eliminate the even harmonics by calculating the following current difference using our previous data of measurements or of Eq. (1):

$$I3 = I_{\mathrm{DS}}(V_{\mathrm{DS}}) - I_{\mathrm{DS}}(-V_{\mathrm{DS}}). \tag{13}$$

Normalization of $I3$ is done in the same way as shown in paragraph 2. The resulting analytical current in normalized variables can be written as:

$$i3(v) = \frac{1}{2}\left[1 + \frac{1-\gamma^2}{1+P\gamma}\frac{1+P\gamma(2v-1)^2}{1-\gamma^2(2v-1)^2}(2v-1)\right]. \tag{14}$$

The normalized $i3$–v curves are shown in Fig. 2, indicating again the excellent agreement between the analytical model of Eq. (14) and the experimental data normalized using Eq. (13). The analysis of the output current calculated from Eq. (14) indicates that there is a non-linearity present, that has an S shape and is symmetrical with respect to $v = 0.5$. If the function D is calculated, his value will be zero. For this reason, the new function $D3$ must be calculated in the interval from $v = 0$ to $v = 0.5$ and the result multiplied by 2, since due to its symmetric behavior the calculus in the whole interval will always be zero.

The resulting function $D3$ is equal to:

$$D3 = 2\left|2\int_0^{0.5} i3(v)\,\mathrm{d}v - 0.25\right|. \tag{15}$$

If the analytical expression for the output current in Eq. (14) is used, the following analytical expression for $D3$ is obtained:

$$D3_{\mathrm{ana}} = \frac{1}{2}\left|1 + \frac{1-\gamma^2}{\gamma^3(1+P\gamma)}\left[P\gamma^2 + (P+\gamma)\ln\left(1-\gamma^2\right)\right]\right|. \tag{16}$$

When γ tends to 0, $D3_{\mathrm{ana}} = 0$, as expected. This result indicates that the term of V_{DS} in the denominator clearly conditions the HD3 magnitude.

5. Correlation of function *D* with THD and of function *D*3 with HD3

To validate our method, the first step was to demonstrate that original and normalized *I–V* characteristics give the same harmonic distortion content. The harmonic coefficients *c*0, *c*2, *c*3, *c*4 and *c*5 were compared by applying the standard FC method to the current obtained from Eqs. (1) and (7), for an input sinusoidal signal of amplitude V_{m} and 1 kHz frequency applied to the drain. Only the DC component, *c*0, differs in a magnitude of 0.5. This difference is caused by the displacement of the curve to the first quadrant, so if the normalized current is used to calculate the zero coefficient harmonic, a value of 0.5 must be subtracted to the result obtained. This result shows that the normalized characteristics can be used in order to determine the harmonic distortion. The THD was calculated for 21 elements including harmonics 0 and from 2 to 20.

The second step was to calculate THD, HD2 and HD3 by the FC method, using the normalized *I–V* measured data and Eq. (7). At the same time, using the same data, function *D* was calculated using Eq. (10).

The last step consisted in calculating HD0, HD2 and HD3, by the FC method applied to the normalized current difference *I*3–*V* measured data and Eq. (14). At the same time, function *D*3 was calculated on the same experimental and model data. Experimental *I–V* data is substituted into Eq. (13) and the resulting current difference is normalized as indicated above. The new resulting data, as well as the *I–V* curve, calculated using Eq. (14), are used to determine each of the above parameters. As expected the values of HD0 and HD2 were always zero.

This procedure was applied to two SOI FD MOSFETs, whose extracted parameters are shown in Table 1. Table 2 summarizes the results of calculations proposed hereabove for these transistors. The gate bias was equal to 1.5 V; back gate voltage $V_{\mathrm{BS}} = 0$ V; $V_{\mathrm{m}} = 0.5$ V and $f = 1$ kHz. Table 2 also includes the harmonic distortion measured for these conditions, using an AC setup with a digital sinus source and a look-in amplifier.

The following remarkable results can be underlined:

1. The ratio between THD and *D* is always constant and equal to 1.06 (0.5 dB).
2. The values obtained for THD, HD2 and *D* are the same whether experimental (column A) or calculated (column B) data are used indicating that the semi-empirical expression used for the calculated data (i.e. Eq. (1)) is a very good approximation in this case.
3. The calculated value for HD3 is the same whether the measured I_{DS}–V_{DS} curve (column A) or the normalized data resulting from Eq. (13) (column C) are used.
4. There is however a significant difference in the values obtained for HD3 if it is calculated using the experimental data (columns A, C) or the analytical expression (columns B, D), indicating that the semi-empirical expression of Eq. (1) is not sufficiently precise in order to calculate the third harmonic. According to Refs. [3,5], a much more physical modeling of the substrate or body effect must be taken into account in SOI FD MOSFETs.
5. Nevertheless, the values obtained for HD3 and *D*3 are exactly the same if the data used for their calculation are either experimental (column C) or calculated (column D).
6. The AC measured (column E) HD2 and HD3, and the DC calculated ones using the experimental data (column A, C), show a good agreement. This demonstrates that the harmonic frequency components can indeed validly be extrapolated from DC *I–V* characteristics, at least up to 1 kHz.

Another important advantage of the new method we propose is that, using functions *D* and *D*3, it is possible to quickly analyze the effect of the applied voltages and parameter variations on the harmonic distortion. The *I–V* characteristic required for calculations can be measured, simulated or calculated analytically. If analytical calculations are used, a more precise model than the one we used, is however required to determine HD3.

Table 2
Distortion parameters THD, HD2, HD3 calculated by FC method and *D*, *D*3 calculated using Eqs. (10) and (15), using normalized data as obtained from (A) experimental $I_{\mathrm{DS}} = f(V_{\mathrm{DS}})$ curve; (B) analytical expression of Eq. (1) with parameters of Table 1; (C) experimental data, $I3 = f(V_{\mathrm{DS}}) - f(-V_{\mathrm{DS}})$; (D) analytical expression of Eq. (14); (E) THD, HD2, HD3 measured in an AC setup

Channel length	(dB)	A	B	C	D	E
2 μm	THD	−16.4	−16.4			
	D	−16.9	−16.9			
	HD2	−19.4	−19.4			−18.6
	HD3	−43.8	−58.3	−43.8	−58.3	−42.6
	*D*3			−43.8	−58.3	
20 μm	THD	−15.9	−15.9			
	D	−16.4	−16.4			
	HD2	−18.9	−18.9			−19.3
	HD3	−55.9	−63.6	−55.9	−63.6	−57
	*D*3			−55.9	−63.6	

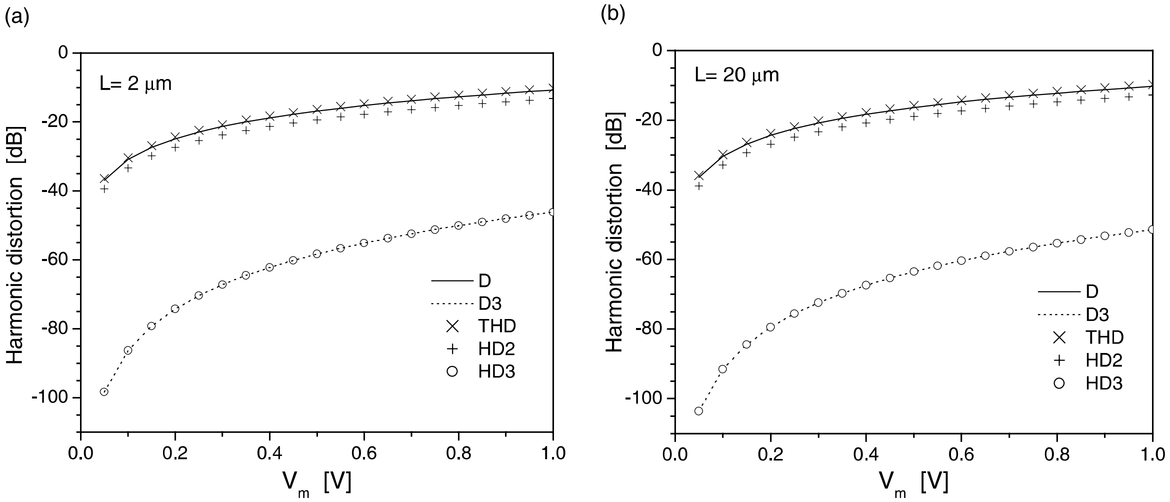

Fig. 3. Variation of *D*, *D*3, THD, HD2 and HD3 with the signal amplitude V_m for $V_{GS} = 1.5$ V and (a) $L = 2$ μm; (b) $L = 20$ μm.

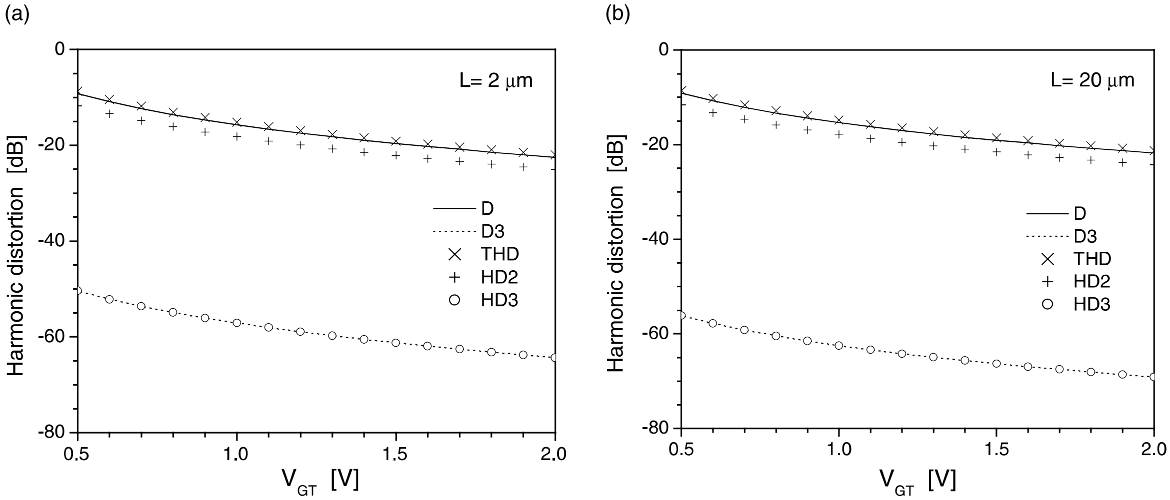

Fig. 4. Variation of *D*, *D*3, THD, HD2 and HD3 with the gate bias $V_{GT} = V_{GS} - V_T$ for $V_m = 0.5$ V and (a) $L = 2$ μm; (b) $L = 20$ μm.

Figs. 3 and 4 show the values obtained for *D*, *D*3, THD, HD2 and HD3, using the analytical expressions of Eqs. (7) and (14) for the two transistors length under consideration. Fig. 3 depicts the expected increased of the harmonic distortion when the amplitude of the sinusoidal signal V_m is varied from 0.05 to 1 V for fixed gate bias. Fig. 4 shows the expected THD, HD2 and HD3 decrease with increasing gate bias in the linear region (V_{GT} varied from 0.53 to 2 V) for fixed V_m. Figs. 3 and 4 thus confirm the excellent correlation of *D* with THD and *D*3 with HD3 in the whole bias range. Furthermore the results also confirm that a V_{GT} of 1.5 V only is sufficient to reduce the HD3 below −60 dB in SOI FD MOSFETs, even for a 1 V peak-to-peak signal amplitude applied between source and drain, on the contrary to comparable bulk Si devices [4,5].

6. Conclusions

We have presented a new method for calculating the THD and the HD3 of a semiconductor device directly from its DC current–voltage characteristic in the operation region of interest. It is based on the use of two integral functions *D* and *D*3. Function *D* is defined as the difference of areas of a normalized *I–V* characteristic. The procedure is simple, precise and does not need the use of complicated FC or FTT calculations or AC measurements. It was demonstrated that there is a constant ratio between THD and function D, equal to 1.06, whereas function $D3$ is exactly identical to HD3. This important result opens up the possibility to quickly analyze the variations of the THD, HD2 and HD3 with applied voltages or different parameters, directly from the DC measured, simulated or modeled I–V characteristics, provided that, in the last case, a sufficiently precise model of the odd-order non-linearities is used.

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